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Issue 6/2009

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FPGAs RESHAPE EMBEDDED DESIGN

Page 38

TAMPER-RESISTANT SMART POWER METERS RELY ON ISOLATED SENSORS

Page 29

WHATEVER HAPPENED TO MY DYNAMIC RANGE?

Page 47

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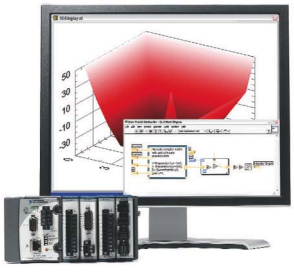

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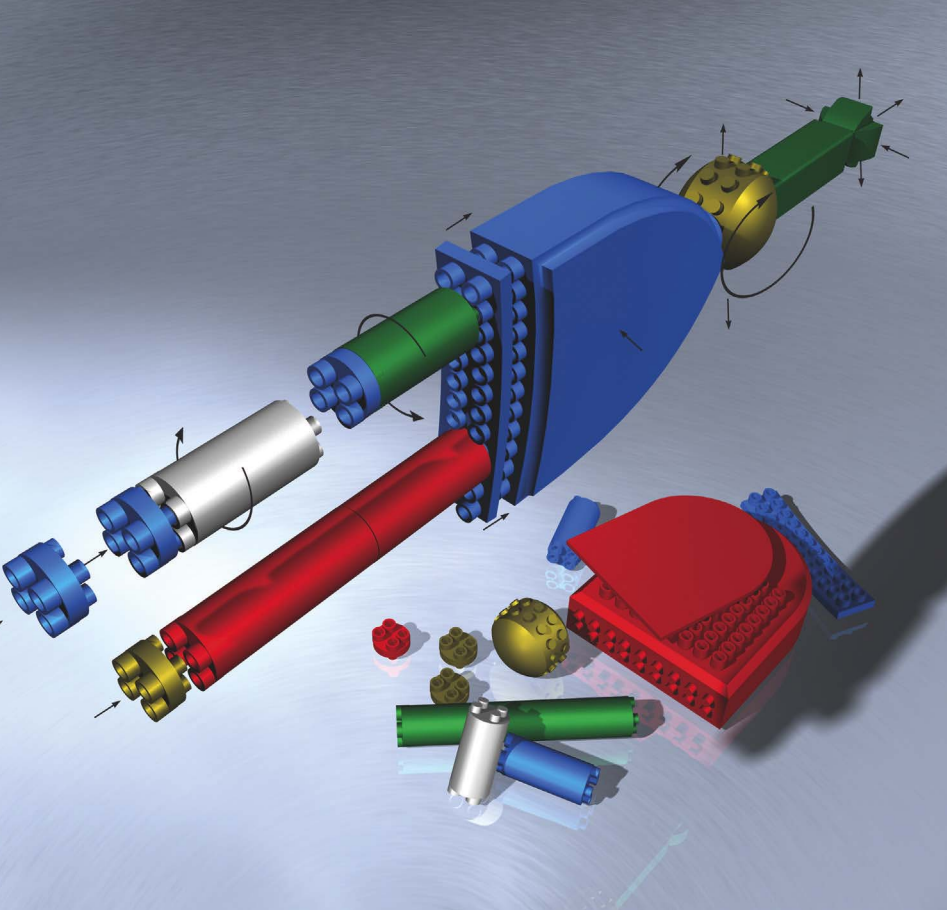


EDN contents

3.19.09

Whatever happened to my dynamic range?

by Steve Green, Cirrus Logic

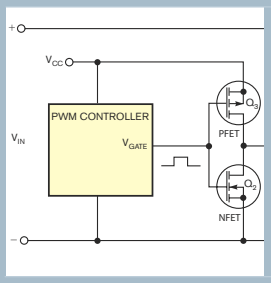
FPGAs reshape embedded design

by Warren Webb, Technical Editor

Tamper-resistant smart power meters rely on isolated sensors

by Margery Conner, Technical Editor

DESIGNIDEAS



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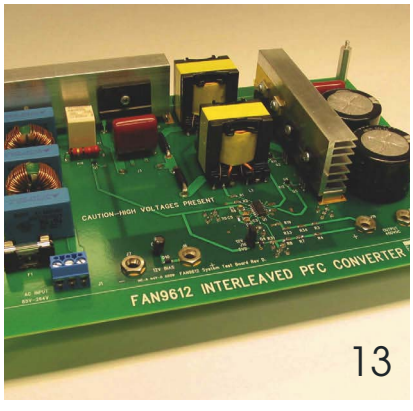

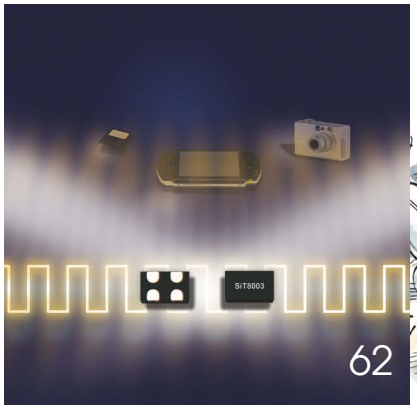

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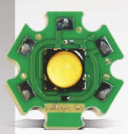

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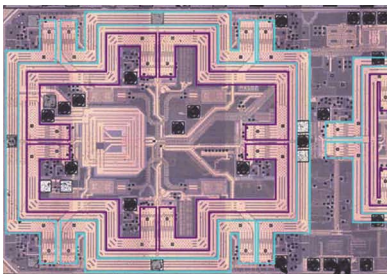

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Tips for designing ultralow-power systems
Follow these tips to save power in battery-powered, microprocessor-based systems.
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FIND YOUR DSP

The online version of *EDN*'s 2009 DSP Directory—a drastically expanded version of what appeared in these pages last issue—is available. The directory allows you to quickly home in on DSP devices and cores that meet your application needs.
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READERS' CHOICE

A selection of recent articles receiving high traffic on www.edn.com.

Verifying FPGA designs: simulate, emulate, or hope for the best?
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First Solar breaks solar energy's $1-per-watt barrier
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A tale of two digital-video converters
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EDN INNOVATION

INNOVATION AWARDS

EDN will announce the Innovator of the Year and the Innovations of the Year at an awards ceremony in San Jose, CA, on March 30. If you can't join us there, check edn.com to find out who took home top honors. Read more about the winners in our April 23 issue.
→www.edn.com/innovation

BY RICK NELSON, EDITOR-IN-CHIEF

Museum contends with multimedia rights

Wherever technology goes, legal issues regarding copyright ownership seem to follow. When law and technology collide, it's often over piracy and DRM (digital-rights management). But it turns out that technology can raise rights issues even when no technological DRM schemes or deliberate attempts at piracy are involved.

One such instance came to my attention on a recent visit to LACMA (Los Angeles County Museum of Art, www.lacma.org). I was there to learn about the prequalification testing the museum and its consultants performed before installing a campus-wide WLAN (wireless local-area network). You can read the details in a related article (**Reference 1**).

One feature of LACMA's WLAN is that it delivers multimedia content to visitors equipped with museum-issued PDAs (personal digital assistants). "Traditionally, museums have audio tours and paper-based content," says Peter Bodell, LACMA's chief information officer. "So, we stepped up and said, 'All right, we need to go to the next level; we need to get it to multimedia.'"

From a visitor's perspective, the implementation is impressive. On arriving at the museum, you can check out a tablet PC. As you stroll about the museum, you can key in three-digit codes near each object that give you access to associated multimedia content. You can listen to audio content while examining similar works on the tablet's screen. As you tour the museum, you can select "favorites." When you get home, you'll have received an e-mailed link to your own virtual gallery, in which you can review your favorites and do more research.

The museum has asked an independent organization to conduct a study of visitor acceptance of the multimedia system, but Jane Burrell, vice president for education and public programs, says that initial indications are favorable. "People love the content," she says. "They've really been excited."

Museum personnel are as pleased with the system as visitors seem to be. "It's a great opportunity for us," says Burrell. "One of the things we hear from our curators all the time is, 'We want to write more. There is so much more we want to say about our objects.' But there is only so much that people can read in the galleries. We have strict guidelines for how much written text we can have in the galleries, and visitors can absorb only so much. But, with the ability to show images, we can tell a different kind of story—one that we couldn't tell with a label."

But telling that different kind of story presents its own challenges, which can be as significant as the technical ones Bodell faced when trying to implement a WLAN that could handle the mix of traffic that PDAs, staff and visitor laptops, and VOIP (voice-over-Internet Protocol) handsets generate.

Content creation is itself a challenge, as Burrell and her staff work to produce multimedia programming for the museum's vast collection. But DRM issues are proving to be particularly challenging. Clearing the rights to use videos has been particularly difficult. "We've had so many people turn us down for video—just small documentary filmmakers who thought, 'OK, this is my chance to get rich,'" she says. "We have only limited funding for the rights, so we've had to say, 'We just can't afford it.'"

Another problem is that many museums that might be willing to share content simply aren't set up to address the rights issues that arise. LACMA staffers calling to request rights, Burrell says, get bounced from department to department, or their calls don't get returned.

And that's too bad. There's no technical solution to the problem. The problem may solve itself as multimedia capabilities expand to many other museums. And that expansion seems inevitable. "A lot of modern artists are starting to work with technology as a medium," Bodell notes. As museums adopt technology to support those artists, it would be the ideal time to provide multimedia content to visitors and to establish procedures for obtaining rights from and granting them to other institutions. Museums and their visitors will be much the richer. EDN

REFERENCE

1 Nelson, Rick, "The art of wireless," *Test & Measurement World*, March 2009, pg 20, www.tmworld.com/article/CA6639355.

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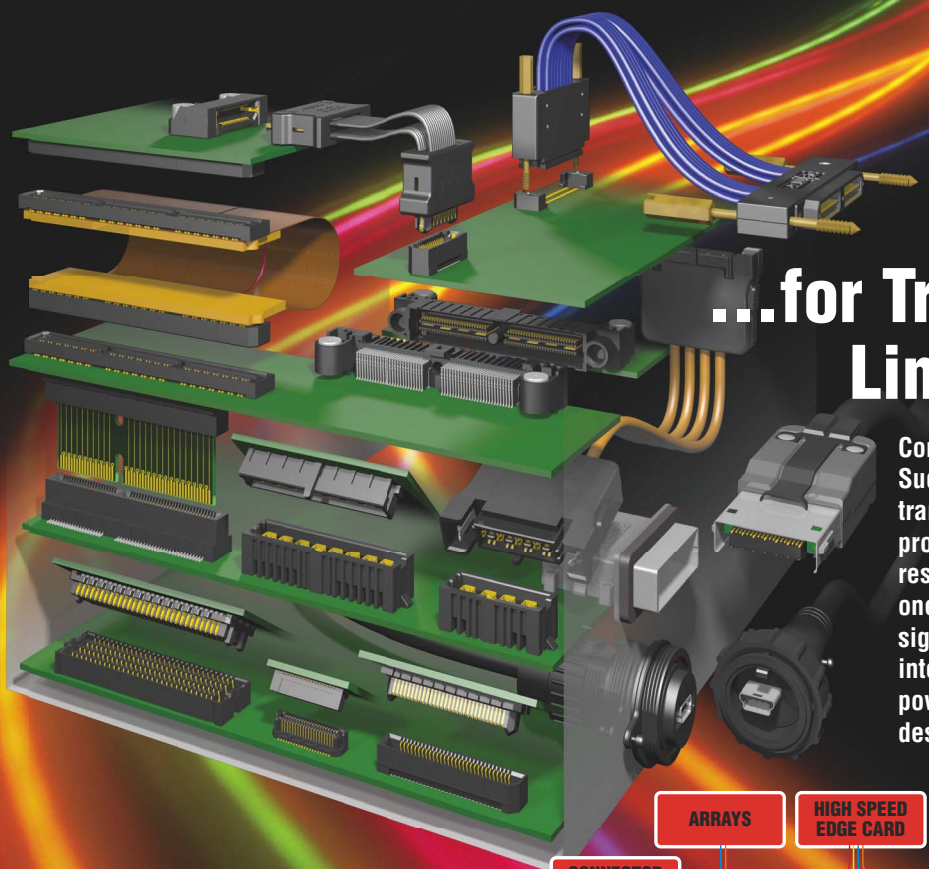

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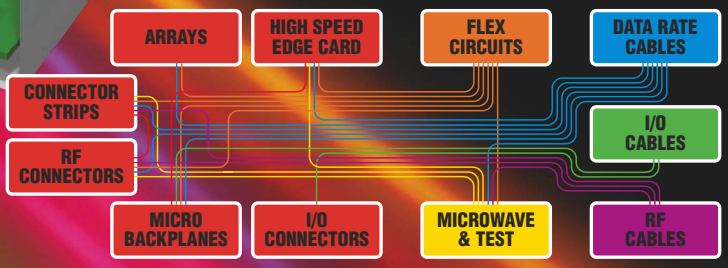

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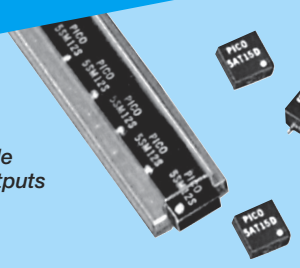

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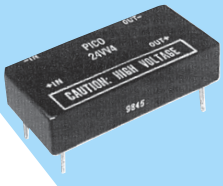

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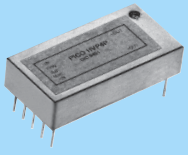

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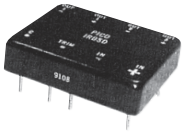

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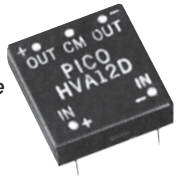

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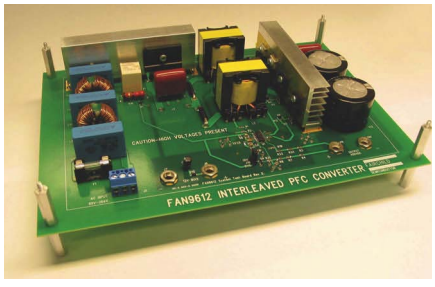
INNOVATIONS & INNOVATORS

PFC controller achieves 96% efficiency

Fairchild Semiconductor has introduced the FAN9612 two-phase BCM (boundary-conduction-mode) PFC (power-factor-correction) controller for 100 to 1000W power systems. Driving external, high-voltage FETs, the device can realize efficiencies of 96% and targets use in two-phase, interleaved PFC control. Dual-phase operation improves efficiency and allows you to reduce the input filter size by 10%.

BCM represents the precise transition point between CCM (continuous-conduction mode) and DCM (discontinuous-conduction mode). In CCM, the PFC inductors continuously carry current; in DCM, the inductors "run dry"—that is, go to zero current—for part of the switching cycle. With BCM, each inductor goes to zero current, and the device then switches back on. The controller can automatically disable one of the two phases when driving light loads to improve efficiency.



The FAN9612 evaluation board gives you a quick start in the design of a dual-phase boundary-conduction-mode PFC power supply.

The device features overcurrent protection and power-limit sensing for each channel, input brownout detection, and input overvoltage protection. You can design in soft start, and the restart operating frequency is above the audio range. The inductor size you select and the input voltage determine a switching speed of 18 to 600 kHz. The device also provides for input voltage feedforward to improve line regulation.

The FAN9612 provides PFC for digital TVs, desktop and entry-level server computers, front-end-telecom systems, and industrial-power systems. It comes in a 16-pin SOIC package, operates in the −40 to +125°C temperature range, and sells for $1.30 (1000).**—by Paul Rako**

▷**Fairchild Semiconductor**, www.fairchildsemi.com.

FEEDBACK LOOP

"It's time the FPGA vendors paid attention to the hardware engineers that carry the water in this industry before we replace FPGAs with multicore SOCs."

—Reader and self-described "hardware guy" Mike Vis, in *EDN*'s Feedback Loop, at www.edn.com/article/CA6633947.

AFS Nano speeds 5000-element design simulations

Berkeley Design Automation has announced its AFS Nano, a version of the company's AFS (Analog FastSpice) with a 5000-element capacity limit that costs only $1900 for a one-year license. Targeting IC-block-level designers using Linux or Solaris platforms, AFS Nano includes Synopsys (www.synopsys.com) HSpice and Cadence Design Systems (www.cadence.com) Spectre netlist support. It also features Cadence Virtuoso ADE (Analog Design Environment) integration. AFS Nano performs ac, dc, noise, transient, sweep, and Monte Carlo analyses.

AFS Nano enables IC designers to design and characterize their blocks at least two times faster than and for a fraction of the cost of other Spice simulators, the company reports, adding that it can deliver foundry-certified true-Spice-accurate waveforms five to 10 times faster than competing simulators for even moderately sized blocks—for instance, those having 1000 elements. The company estimates that engineers use 50% of Spice simulators for block-level runs that would comfortably fit within AFS Nano's capacity limit. (For more on AFS, which supports 1 million-element analog, mixed-signal, and RF designs, see "Simulation gets speed, capacity boost," *EDN*, Jan 22, 2009, pg 26, www.edn.com/article/CA6629472.)**—by Rick Nelson**

▷**Berkeley Design Automation**, www.berkeley-da.com.

DDR3 test suite features 2G transfer/sec logic-state analysis

Agilent Technologies has introduced a comprehensive DDR (double-data-rate) 3 protocol-debugging and validation-test suite for digital-system designers who develop computer and embedded-memory applications. The test platform includes the 2-GT/sec (gigatransfer/sec) 16962A plug-in logic-analysis module for the company's 16901A and 16902A logic-analyzer mainframes. The test suite also includes a probing portfolio for DDR3 BGAs (ball-grid arrays) and DIMMs (dual-in-line memory modules) and a DDR3-compliance and -performance-measurement environment.

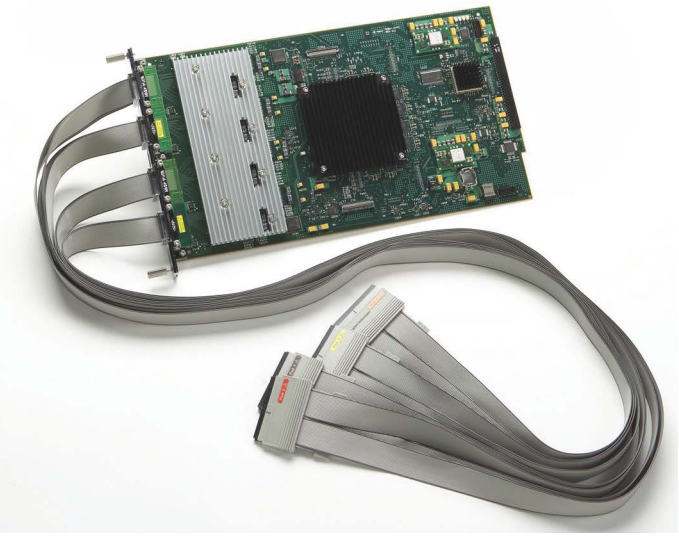
The test suite enables research and development engineers who integrate memory controllers with the DDR-memory devices in the memory subsystem to perform interoperability testing. This testing is a major challenge for many designers because manufacturers often develop the memory-controller design in-house and integrate it with IP (intellectual property) they acquire from third parties.

Within the past year, the use of DDR3 has significantly increased in both computers and embedded-memory designs because DDR3 devices provide higher performance and consume less power than do previous-generation DDR2 devices. To ensure that the technology is testable, engineers must take into account test-and-measurement requirements when they write specifications for complex, high-speed computer systems. Measurements are central to diagnosing problems and proving that the corrections to those problems work correctly. By contributing to standards groups, such as JEDEC (Joint Electronic Device Engineering Consortium), Agilent ensures that new designs are testable and guarantees that the company's products ensure specification compliance.

> The probes work with oscilloscopes and logic analyzers to perform physical-layer and functional tests.

The DDR test suite, which includes the $38,135 16962A module with 4 million-pattern memory, 2-GT/sec state speed, and 2-GHz trigger-sequence speed, reliably triggers on and captures 1.6-GT/sec DDR3 1600 signals. When designers use this module with the new DDR3 probing system and analysis software, it provides full test capability for system integration in the memory industry. On embedded-system designs, the W3630A-series DDR3 BGA probes, with prices starting at $400, provide direct access to the DRAM contacts with low capacitive loading and minimal impact on signal integrity. The probes work with oscilloscopes and logic analyzers to perform physical-layer and functional tests. In server and desktop applications, the $40,800 N4835A DDR3-slot interposer enables nonintrusive memory-bus access through a slot connector at speeds to 1.6 GT/sec. The slot interposer provides quick and easy access to industry-standard DDR3 DIMMs, including 240-pin packages.

In addition to announcing an ensemble of DDR-testing hardware tools, Agilent introduced what it calls the industry's first DDR2 and 3 protocol-compliance and analysis software tool, the $5500 B4622A, which will help to reduce memory designers' troubleshooting time and increase productivity and efficiency in DDR-design validation. This tool, which works with all of the manufacturer's current DDR2 and 3 test equipment, provides timing and protocol-violation checks, automated physical-address-trigger setup, and an overview of system performance through bus-statistic information and a histogram view of address access.**—by Dan Strassberg**
▷**Agilent Technologies**, www.agilent.com/find/ddr.



The 68-channel 16962A module, which plugs into the manufacturer's logic-analyzer mainframes, triggers on and captures DDR3 bus transactions at 2G transfers/sec in the state-analysis mode.

DILBERT By Scott Adams

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Lithium-ion cell-measurement instruments offer 48 24-bit-resolution inputs

Data Translation has announced its Voltpoint series of voltage-measurement instruments for lithium-ion cell-by-cell determination. Each Voltpoint is a stand-alone box offering 48 24-bit-resolution inputs over a sampling range of ±100V, each with its own sigma-delta ADC for direct connection to a PC through USB or Ethernet. The LXI (LAN-extensions-for-instrumentation)-compatible instruments can make high-voltage, high-precision battery-stack and cell-balance measurements in commercial and military hybrid-vehicle applications. They accept direct voltage inputs of any value in the range of ±100V from a single cell or from a series of stacked cells. In addition, the instruments can make motor-shunt measurements. Each of the 48 input channels offers 1000V channel-to-channel galvanic isolation. Maximum error is 3 mV for any input range.

The Voltpoint series of voltage-measurement instruments for lithium-ion cell-by-cell determination offers 48 24-bit-resolution inputs over a sampling range of ±100V, each with its own sigma-delta ADC for direct connection to a PC through USB or Ethernet.

Channels operate simultaneously at throughput rates as high as 10 Hz per channel. The instruments feature 16 optoisolated digital-I/O lines—eight input lines and eight output lines—for monitoring and driving relays. Voltpoint instruments feature eight isolated digital-input lines that operate from 3 to 28V dc, with a maximum switching time of 2 msec. The instruments can directly drive relays using eight isolated digital-output lines. The outputs incorporate solid-state relays that operate at ±30V and 400 mA peak ac or dc with a maximum switching time of 2 msec. The digital-I/O lines feature channel-to-channel isolation as great as 250V between digital-I/O lines. Using every other line doubles the isolation but halves the number of usable I/O lines. The instruments support software triggering to initiate measurements.

The instrument comes with the software necessary to enable measurements as soon as you take it out of the box. The vendor offers software supporting the Voltpoint, including IVI-COM (interchangeable-virtual-instrument-communication) drivers, .NET class libraries, and software-development kits. Voltpoint is available in the DT9873 version for USB, which costs $7995, and the DT8873 version for Ethernet LXI, which costs $8495. Data Translation has begun shipping both versions.**—by Rick Nelson**

▷**Data Translation**, www.datatranslation.com.

DSP CORE SUPPORTS 4G WIRELESS INFRASTRUCTURE

Ceva's Ceva-XC DSP core employs the company's Ceva-X architecture to support 3.5 and 4G wireless designs. The new architecture accommodates one, two, or four vector-communication units alongside a single general computational unit to provide hardware support for as many as 64 simultaneous 16×16-bit MAC (multiply/accumulate) operations or 128 16×8-bit MAC operations when using all four vector units. Each vector unit is a 256-bit SIMD (single-instruction/multiple-data) engine using a three-way VLIW (very-long-instruction-word) architecture that supports as many as three parallel instructions, with each instruction operating on 256-bit registers.

Each engine can incorporate optional instruction sets to better balance between performance and cost to support transmitter functions, floating-point operations, and the CORDIC (coordinate-rotation-digital-computer) algorithm. Additional advanced hardware includes support for MIMO (multiple-input/multiple-output) detectors; channel estimation; and bit-chain processing for interleavers, scramblers, and FEC (forward-error-correction) encoders.

The execution units combine with the memory subsystem to enable a software implementation for LTE (long-term-evolution) Class 5 or WiMax (worldwide-interoperability-for-microwave-access) II designs that must support a downlink data rate of 300 Mbps with 4×4 MIMO. The memory subsystem employs AXI (advanced-extensible-interface) master and slave system buses that are configurable between 64- and 128-bit widths, and it includes an APB (advanced-peripheral-bus) 3 interface to support slow devices.

The memory subsystem supports caches; tightly coupled memories; and interfaces for emulation, profiling, and real-time trace modules. It supports optional EEC (extended error correction) for memory error detection and correction. The DMA (direct-memory-access) engine supports 2-D transfers that can operate in background data transfers and data-rate-matching modes.

For an expanded description of this product, go to www.edn.com/090319pa.—by Robert Cravotta

▶**Ceva, www.ceva-dsp.com.**

03.19.09

LINEAR TECHNOLOGY

DESIGN NOTES

100V Controller Drives High Power LED Strings from Just about Any Input – Design Note 461

by Keith Szolusha

Introduction

Strings of high power solid-state LEDs are replacing traditional lighting technologies in large area and high lumens light sources because of their high quality light output, unmatched durability, relatively low lifetime cost, constant-color dimming and energy efficiency. The list of applications grows daily, including LCD backlights and projection, industrial and architectural lighting, automotive lights, streetlights, billboards and stadium lights.

As the list expands, so does the range of V_{IN} for the LED drivers. LED drivers must be able to handle wide ranging inputs, including transient voltages of automotive batteries, a wide range of other batteries and wall wart voltages. For LED lighting manufacturers, applying a different LED driver for each application means stocking, testing and designing with a number of controllers. It would be better to use just one that can be applied to many solutions.

The LT3756 high voltage LED driver features a unique topological versatility that allows it to be used in boost, buck-boost mode, buck mode, SEPIC, flyback and other topologies. Its high power capability provides potentially hundreds of watts of LED power over a wide input voltage range. Its 100V floating LED current sense inputs provide accurate LED current sensing. Excellent PWM dimming architecture produces high dimming ratios.

A number of features protect the LEDs and surrounding components. Shutdown and undervoltage lockout, when combined with analog dimming derived from the input, provide the standard ON/OFF feature as well as a reduced LED current should the battery voltage drop to unacceptably low levels. Analog dimming is accurate and can be combined with PWM dimming for a wide range of brightness control. Soft-start prevents spiking inrush currents. The $\overline{\text{OPENLED}}$ pin informs of open or missing LEDs and the SYNC (LT3756-1) pin can be used to sync switching to an external clock. The FB voltage loop limits the max V_{OUT} to protect the converter in the case of open LEDs.

The 16-pin IC is available in a tiny QFN (3mm × 3mm) and an MSE package, both thermally enhanced. For lower input voltage requirements, the $40V_{IN}$, $75V_{OUT}$ LT3755 LED controller is a similar option.

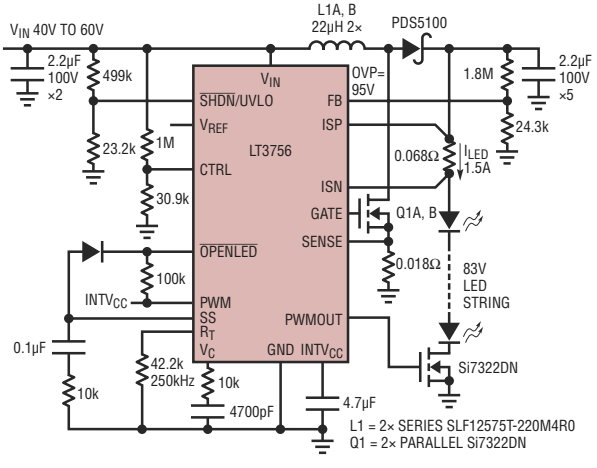

Figure 1. A 125W, 83V at 1.5A, 97% Efficient Boost LED Driver for Stadium Lighting

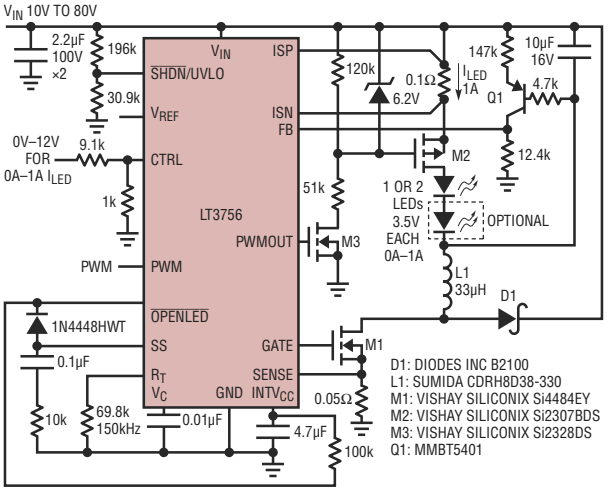

Figure 2. An $80V_{IN}$ Buck Mode LED Driver With PWM Dimming for Single or Double LEDs

Boost

Lighting systems for stadiums, spotlights and billboards require huge strings of LEDs running at high power. The LT3756 controller drives up to 100V LED strings. The 125W LED driver in Figure 1 has a 40V–60V input.

The high power gate driver switches two 100V MOSFETs at 250kHz. This switching frequency minimizes the size of the discrete components while maintaining high 97% efficiency, producing a less-than-50°C discrete component temperature rise—more manageable than the heat produced by the 125W LEDs.

Even if PWM dimming is not required, the PWMOUT MOSFET is useful for LED disconnect during shutdown. It prevents current from running through the string of LEDs.

If the LED string is removed, the FB constant-voltage loop takes over and regulates the output at 95V. Without overvoltage protection, the LED sense resistor would see zero current and the output cap voltage would go over 100V, exceeding several max ratings. While in OVP $\overline{\text{OPENLED}}$ goes low.

Buck Mode

When V_{IN} is higher than V_{LED}, the LT3756 can serve equally well as a buck mode LED driver. The buck mode LED driver in Figure 2 operates with a wide 10V-to-80V input range to drive one or two LEDs at 1A.

PWM dimming requires a level-shift from the PWMOUT pin to the high-side LED string. The max PWM dimming ratio increases with higher switching frequency, lower PWM dimming frequency, higher V_{IN} and lower LED power. In this case, a 100:1 dimming ratio is possible with a 100Hz dimming frequency and a 48V input. Although higher switching frequency is possible, the duty cycle has its limits. Generous minimum on-time and minimum off-time restrictions require a frequency on the lower end of its range (150kHz) to meet both the harsh high-V_{IN}-to-low-V_{LED} ($80V_{IN}$ to one 3.5V LED) and low-V_{IN}-dropout requirements ($10V_{IN}$ to $7V_{LED}$).

OVP of the buck mode LED driver has a level shift as well. Without the level-shifted OVP network tied to FB, an open LED string would result in the output capacitor charging up to V_{IN}. Although the buck mode components will survive this scenario, the LEDs may not survive being plugged into a potential equal to V_{IN}.

Buck-Boost Mode

A common LED driver requirement is that the ranges of both the LED string voltage and the input voltage are wide and overlapping. In fact, some designers prefer to use the same LED driver circuit for several different battery sources and several different LED strings. Such a versatile configuration trades some efficiency, component cost, and board space for design simplicity, and time-to-market.

The buck-boost mode driver in Figure 3 uses a single inductor. It accepts inputs from 9V to 36V to drive 10V–50V LED strings at 400mA.

The inductor current is the sum of the input current and the LED string current; the peak inductor current is equal to the peak switching current. Below 9V input, CTRL analog dimming scales back the LED current to keep the inductor current under control. UVLO turns off the LEDs below $6V_{IN}$. C_{OUT}, DI and MI can see voltages as high as 95V here.

Conclusion

The LT3756 controller is a versatile high power LED driver. It has all the features required for large (and small) strings of high power LEDs. Its high voltage rating, optimized LED driver architecture, high performance PWM dimming, host of protection features and accurate high side current sensing make the LT3756 a single-IC choice for a variety of lighting systems.

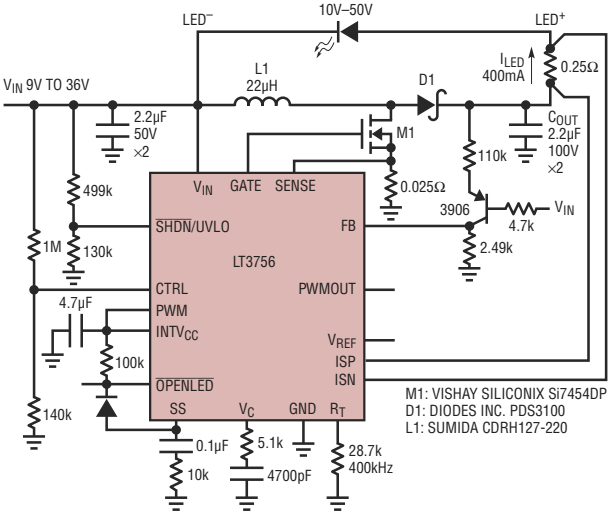

Figure 3. A Buck-Boost Mode LED Driver With Wide-Ranging V_{IN} and V_{LED}

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One radio-test platform addresses development, production environments

Rohde & Schwarz has announced a wideband-radio-test system that the company based on its 6-GHz CMW500 radio-test set. The new system will provide a single platform for both development and production-test environments, and it spans all significant cellular and noncellular standards. The company aims to provide wireless-devices makers, baseband- and RF-chip-set providers, and network operators with a stable test system that will operate over many years.

As a wideband-radio tester, the single-chassis unit tests all layers from RF parametric measurements to protocols and applications. The CMW500 is a modular instrument, and the new platform will be modular in both hardware and software.

The unit combines RF-generator and RF-analyzer functions. It supports GSM (global-system-for-mobile)-communications Europe/GPRS (general-packet-radio-service), WCDMA (wideband-code-division/multiple-access)/HSPA (high-speed-packet-access), LTE (long-term-evolution), TD-SCDMA (time-division-synchronous-code-division-multiple-access), CDMA2000 1×RTT (one-times-radio-transmission-technology), CDMA2000 1×EVDO (one-times-evolution-data-optimized), Mobile WiMax (worldwide-interoperability-for-microwave-access), WLAN (wireless-local-area-network), Bluetooth, DVB-T (digital-video-broadcasting-terrestrial), and GPS (global-positioning-system) standards. Multitechnology support handles test cases, such as handover and cell-selection procedures, in which multiple standards are in play.

In contrast to such layered development-test scenarios, in production test, you can configure the same basic platform to optimize it for minimum test time and, hence, cost. The company's Smart Alignment concept cuts alignment times by as much as 90%, and the unit's two complete channels allow parallel measurements to take place on two products—which need not employ the same standard. Using a single platform means that you can easily transfer to production test scripts you create in development.

Sending high data rates over nonideal radio channels involves complex protocol-layer processes; the mobile must correct data packets with errors and handle multiple data streams in parallel. These fast processes, such as HARQ (hybrid automatic repeat request) and MIMO (multiple input/multiple output), run at layers 1 and 2 and require a tester that simultaneously performs protocol analysis and hardware-oriented RF measurements.

According to Anton Messmer, director of the company's mobile-radio-tester subdivision, in the early stages of working with a standard, you would have previously required a protocol tester and RF parametric measurements. Now, he says, one unit provides all the data and performs end-to-end testing of the complete communications link in realistic signal environments. Despite the economic downturn, cellular operators are still pressuring the company's leading customers to have LTE products ready for a 2010 rollout, Messmer adds. Increasingly, testing will encompass end-to-end systems measurements, such as real data rate and even battery life.**—by Graham Prophet**

▷**Rohde & Schwarz**, www2.rohde-schwarz.com.

The CMW500 wideband-radio-test system handles wireless-test tasks.

MEZZANINE MODULE USES FPGA TECHNOLOGY

03.19.09

Curtiss-Wright Controls Embedded Computing recently announced an I/O-mezzanine COTS (commercial-off-the-shelf) card that combines a user-programmable FPGA and configurable I/O in a PMC (peripheral-component-interconnect-mezzanine-card)/XMC (extended-mezzanine-card) form factor for applications such as imaging, system control for radar, software-defined radio, and signal-intelligence platforms.

The XMC-FPGA05D combines reconfigurable-FPGA processing with high-speed datapaths.

The XMC-FPGA05D includes an onboard Virtex-5 FPGA to control the I/O interface and deliver as many as 138 signals, including signals for ADC, DAC, Camera Link, RS-485, and LVDS (low-voltage differential signaling), from its front panel and as many as 64 signals from the backplane through the host card. Prices for the XMC-FPGA05D start at $7250.

For an expanded description of this product, go to www.edn.com/090319pb.

—by Warren Webb

▶**Curtiss-Wright Controls Embedded Computing, www.cwcembedded.com.**

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ANALOG DEVICES

VOICES

Chip design in recession: a view from an ASIC consolidator

There is no question that the recession, no matter what its future, is profoundly changing IC design. Investment patterns are changing, imposing huge and wrenching changes on engineers. And there are signs that the underlying models of the industry—integrated-device manufacturers, fabless-IC companies, and foundries—may change as well before we get through these trying times. Jack Harding, veteran of the design-automation and ASIC businesses and now at the helm of eSilicon, recently discussed changing times, changing models, and what they might all mean for designers. A portion of that discussion follows. For the full interview, go to www.edn.com/090319pc.

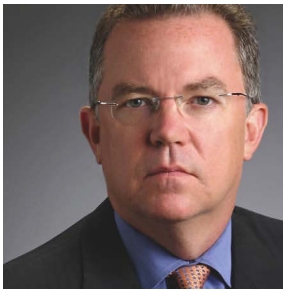
What do you mean when you say that business models are in transition?

A We're seeing executives revisiting all forms of fixed costs on their income statements. These are often companies that have already decided to go fabless, have outsourced back-end design, and [trimmed] their design teams. Now, they are starting to look at operations costs.

If a company is doing one chip design every 18 months, why would [it] keep an operations staff on the payroll? That [move] would be like keeping a full-time staff for mergers and acquisitions. So, we are seeing executives starting to ask, "Can someone take over production management for us?"

And ASIC consolidators can offer that benefit?

A We are basically an aggregator, but maybe we are best known as a fabless-ASIC company. Because we handle lots of designs per month, we very quickly get up the learning curve on back-end



design of new nodes. Instead of each new design's being a new experience, we are able to develop a fairly automated methodology at a new node. We are doing mostly 40- and 45-nm designs, for instance. At this stage, we are tuning the methodology to a manufacturing experience: working on yield and reliability optimization, where we can and cannot compromise with the foundry on design rules—things that come from experience.

But customers have taken us beyond just the design space. Because we are such a large customer to the foundries we work with, we have economies of scale and influence, and we are also skilled in managing product life cycles. As fabless companies understand this point, they see the possibility of changing the business model.

Basically, we can offer to take over responsibility for production on an existing product, deliver the chips to you at the price you have today, and meet the goals on your cost-reduction road map. And we can make money doing that.

In addition to looking at outsourcing operations, are you seeing the fabless-semi companies and system houses looking for other economies, such as postponing designs?

A We are seeing every possible form of cash conservation. Companies are taking designs to RTL [register-transfer-level] freeze and then shelving them. They are delaying tape-outs. They are cutting wafer orders. The paradox of all this is that we as an industry are managing our resources better than we ever have before, but we are still seeing the worst situation.

The good news is that, because of all the attention the industry has paid to inventories since the Internet bubble, we may be in a better position than in the past. Companies we talk to expect to purge their inventories in one to three quarters, not two years.

And design doesn't come to a stop. Companies are still conducting R&D, and they are still doing algorithm development. One thing that might change, though, is the shocking amount of overdesign that has been common in the industry. Design teams may have used 65 nm for a design that would have worked just fine in 90 nm. They might have specified 600 MHz just for head room when the requirements were only 450 MHz. We may see a lot of that overdesign evaporating now as companies try to reduce their NRE [nonrecurring-expense] levels.

Reducing NRE–that must be music to the ears of FPGA companies.

A You know, this is the fourth major recession since the introduction of FPGAs, and their use model still hasn't changed. They are still a small fraction of the size of the ASIC/SOC [application-specific-integrated-circuit/system-on-chip] business. I think perhaps some people have misunderstood that [idea] because chip-design starts have been dropping, but that drop has been primarily because, with increased integration, one SOC will do what 10 ASICs used to do. The drop is not primarily because of FPGAs' displacement of ASICs.

Reality is that, today, if you can reduce the cost of a chip by 50 cents, that is justification enough to replace it in the bill of materials. In that kind of environment, you are not going to pay a huge premium for an FPGA.

Do you see the recession accelerating dispersal of design teams around the world?

A No. Design teams will continue to outsource portions of the design, but we maintain that at a certain level of complexity, proximity of the lead engineers to each other and to the customer is absolutely vital. Dispersing tasks to outlying teams works only when there will be only low interactivity with the remote team and little or no customer involvement in that portion of the design.

—Interview conducted and edited by Ron Wilson

RAQ's

Rarely Asked Questions

Strange stories from the call logs of Analog Devices

Impedance Measuring Chip Offers Little Resistance to Applications

Q: I came across your Impedance measuring chip (IMC) in a recent article. It sounds interesting, but how does it work and what can it be used for?

A: The impedance measuring chip you mention is an extremely versatile device with countless practical applications.

Able to measure complex impedances from 100Ω to 10MΩ with 0.5% accuracy, the IMC is a marvelous example of integration, elegance and practicality. The IMC comprises a direct digital synthesis (DDS) frequency generator, a 12-bit analog-to-digital converter (ADC), and a digital-signal-processing (DSP) engine.

The frequency generator provides a voltage stimulus to the device under test (DUT) at frequencies between 1 kHz and 100 kHz, and the ADC samples the resultant current. The DSP performs a discrete Fourier transform (DFT) on the digitized signal, and produces real (R) and imaginary (I) data words at each frequency. Using this information, the magnitude and phase can be calculated along any point in the frequency sweep.

Limited only by the imagination, some applications for an IMC include virus detection, blood coagulation monitoring, electro-impedance spectroscopy, and loudspeaker optimization.

Different virus strains cause different chemical reactions in blood. Characterizing these reactions by measuring their impedance over frequency enables researchers to identify different virus strains by their impedance signature.

Blood clotting time can be determined by measuring the impedance as it coagulates. Crucial to recovery of heart bypass patients, monitoring coagulation enables doctors to maintain a balance between bleeding and clotting.

Electro-impedance spectroscopy uses impedance to measure corrosion of aluminum and steel in infrastructure, cars, planes, and ships, preventing early failures and unneeded repairs. Impedance measurement chips can be placed in remote, hard to reach spots. This constant "structural supervision" signals maintenance crews to the first sign of corrosion or premature wear.

Measuring speaker impedance across the audio frequency range enables designers to actively match the speaker impedance to the audio driver for optimal performance and power transfer.

It's almost maple sugar season here in New England. I wonder if an IMC could measure the sugar content of the sap… hmm, I'll have to look into that.

To Learn More About Impedance Measurement Applications
http://designnews.hotims.com/23098-101

Contributing Writer John Ardizzoni is an Application Engineer at Analog Devices in the High Speed Linear group. John has been with Analog Devices since 2002, he received his BSEE from Merrimack College in N. Andover, MA and has over 29 years experience in the electronics industry.

Have a question involving a perplexing or unusual analog problem? Submit your question to: raq@reedbusiness.com

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BY BONNIE BAKER

Understanding FFT plots

You can generate an FFT (fast-Fourier-transform) plot by periodically collecting a large number of conversion samples from the output of an ADC. Typically, ADC manufacturers use a single-tone, full-scale analog input signal for the performance curves in product data sheets. You take data from these conversions and create a plot similar to the one in **Figure 1**. The frequency scale of this plot is always linear, from zero to the converter's sampling frequency divided by two.

You generate the plot by applying a sampling frequency of 100k samples/sec to a 12-bit ADC with an analog input signal of 9.9 kHz. The signal at 9.9 kHz is the fundamental input signal (A). The fundamental input-signal spur reaches almost 0 dB.

The specifications of interest in an FFT plot are the fundamental input signal, the SNR (signal-to-noise ratio), the THD (total harmonic distortion), and the average noise floor. A useful way of determining noise in an ADC circuit is with the SNR (B), the ratio of signal power to noise power. The SNR of the FFT calculation is a combination of several noise sources, including the quantization error of the ADC, the internal noise of the ADC, noise from the voltage reference, and noise from the driving amplifier. The theoretical limit of SNR is 6.02n+1.76 dB, where n is the number of converter bits.

The THD (C) quantifies the amount of distortion in the system. The THD is the ratio of the root-mean-square sum of the powers of the harmonic components, or spurs, to the input-signal power. Spurs resulting from the nonlinearity of the ADC appear as whole-number multiples of the input signal's frequency, or fundamental frequency. Most manufacturers use the first seven to nine harmonic components in their THD calculations.

If the ADC creates spurs, it most likely has some INL (integral nonlinearity) errors. Spurs can also come from the input signal through the signal source or the driving amplifier. If the driving amplifier is the culprit, it may have crossover distortion, be unable to drive the ADC, or be bandwidth-limited. Injected noise from other places in the circuit, such as digital clock sources or the mains frequency, can also create spurs in the FFT result.

In an FFT representation of converter data, the average noise floor (D) is a root-mean-square combination of all the bins within the FFT plot but excludes the input signal and signal harmonics. You should choose the number of samples versus the number of ADC bits so that the noise floor is below any spurs of interest. With these considerations in mind, the theoretical average FFT noise floor is 6.02n+1.76 dB+10 log[(3×M)/(π×ENBW)], where M is the number of data points in the FFT, ENBW is the equivalent noise bandwidth of the window function, and n is the number of bits of the ADC. A reasonable number of samples for the FFT of a 12-bit converter is 4096. EDN

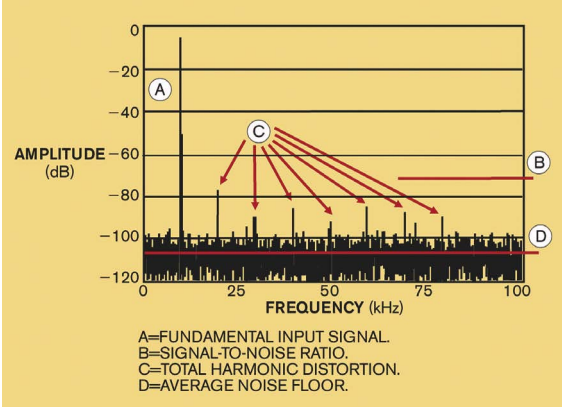

Figure 1 There are 4096 data samples from a 12-bit converter in this FFT plot. The frequency spectrum for a 4096-point FFT is 100 kHz with f_{IN}=9.9 kHz.

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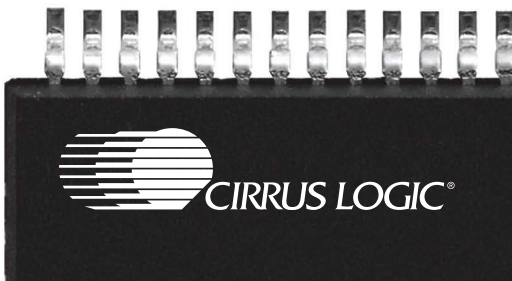

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One sensor does the work of many

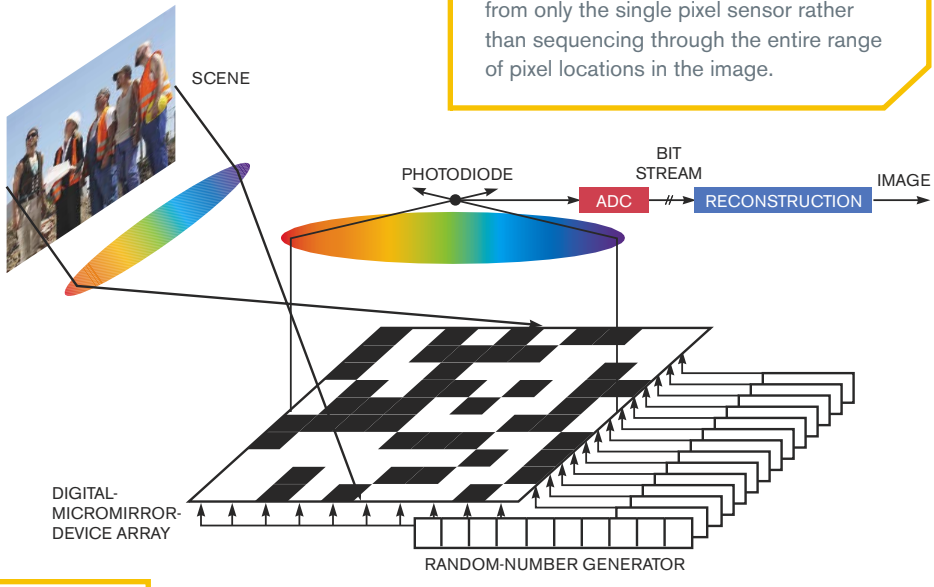
Digital cameras, still relatively inexpensive devices, have exponentially increased the number of pixels they can capture. Because silicon, a primary material in CCD (charge-coupled devices) and CMOS imagers, is sensitive to the same wavelengths as the human eye, digital cameras have been able to double their pixel resolution roughly in step with the doubling in memory sizes.

Rice University is now demonstrating a camera that uses a single sensor to capture images that conventionally require an array of sensors (image courtesy Richard Baraniuk, Rice University). The researchers direct a captured image at a single sensor and use the resulting stream of measurements to reconstruct the image. They accomplish this task without making individual measurements of each pixel.

The second lens captures the reflected light from the DMD array and focuses all of the light to a single pixel-sensor collector. Because all of the reflected light goes toward the sensor, it effectively receives a summation of all of the reflected light. This approach differs from a conventional sensor array in which each pixel sensor receives only a fraction of the total light because each one receives only the light corresponding to a specific pixel location.

The analog-to-digital-conversion step is simpler because the system converts data from only the single pixel sensor rather than sequencing through the entire range of pixel locations in the image.

The system sends the image through a lens much as a conventional camera does; however, instead of directing the light from the captured image to an array of sensors, the light goes to a Texas Instruments (www.ti.com) DMD (digital-micromirror-device) array that comprises bacterium-sized mirrors that correspond in position to the pixels in a conventional image.



TI based the DMD on its DLP (digital-light-processing) technology, which digital televisions and projectors typically use. Using a pseudorandom-number generator, the system configures a random set of half the DMDs in the array so that they reflect the incoming light to a second lens. The remaining DMDs reflect none of the light directed toward them. Each image snapshot uses a different random mix of reflecting and nonreflecting positioning of the DMD.

By tracking the random, half-reflecting-DMD-array configuration with the detected summation of light at the single-pixel sensor, the system applies a compressive-sensing-recovery algorithm across a series of snapshots to reconstruct the image. With this approach, the number of measurements of the scene necessary for adequate reconstruction of the image is only, say, 10, 20, or 40% of the total number of pixels in the image. A seed value for the pseudorandom-number generator manages the random configuration of the DMDs. The system uses this seed value to reconstruct and associate each configuration of the DMD array with the reflected-light-summation value.

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TAMPER-RESISTANT SMART POWER METERS RELY ON ISOLATED SENSORS

BY MARGERY CONNER • TECHNICAL EDITOR

Most residences and commercial buildings in the United States currently use an old-style electromechanical utility power meter to track electricity use. The meters are reliable and cheap but hopelessly inadequate for use by a power-distribution system that requires accurate, repeatable power metrics as well as wired or wireless communications—in other words, the coming Smart Grid electrical-power-distribution system.

The Smart Grid depends on smart meters with sophisticated communication capabilities to monitor energy usage and allow residential and business consumers alike to make informed choices about how much energy to use and when to consume it. The Smart Grid faces difficulties, though. Although, at the federal level, Washington has passed legislature such as the 2007 energy bill and the 2009 stimulus plan, utilities actually deploy power on a state-by-state basis. California and Texas are the states most aggressively moving toward smart metering in preparation for the Smart Grid (**Reference 1**).

Regardless of whether the Smart Grid in some form will proceed at the national level smoothly and seamlessly, enough individual utilities are purchasing and installing electronic power meters to make this market significant. Look at the important applications of the past 20 years: cell phones, computers, large-screen TVs. They make their mark because they have a market in the hundreds of millions. Utility-installed power meters have a similarly powerful market. Every house and commercial building requires one. Utility companies could replace 500 million meters worldwide over the next 10 years.

Smart power meters comprise a mi-

crocontroller with onboard ADC and DAC, a sense component for both voltage and current, an ac/dc-power converter, battery backup, and wireless or wired communication capability (**Figure 1**).

Power-meter ICs are available from companies including Texas Instruments, On Semiconductor, Maxim, Analog Devices, Teridian, and Ev2. These ICs are essentially microcontrollers that track power-usage information as well as information back from the utility. They can perform some DSP calculations on voltage waveform and quality, communicate the information to a display, and store the information to be sent. Although the term *smart meter* indicates that the microprocessor is the central component, antitampering precautions make selection of the current-sensing component and even power backup important decisions for smart meters.

There are three main types of current-sensor technology for power meters: current transformers, Rogowski coils, and resistive shunts. The technology you use depends on whether the power distribution is multiphase or single-phase. Most homes worldwide use only one phase from the generator coming to the wiring of the house. The US residential market uses a split-phase distribution that delivers 120V ac and as much as 240V ac to residences and requires a current transformer as the isolated voltage/current sensor. Commercial and some residential deployments in northern Europe use three-phase, but homes are usually single-phase. In general, when sensing voltage and current to determine power usage in metering, you use a shunt resistor on single-phase distribution systems and a current transformer or Rogowski coil in a split- or three-phase system, because measuring the voltage across different phases can exceed the voltage tolerance of semiconductor devices.

The most popular isolated sensors are current transformers, Rogowski coils, and Hall-effect sensors, roughly in order of popularity (**Figure 2**). A current transformer has an iron core and is susceptible to tampering with a large permanent magnet. A magnet next to the transformer can saturate the core so that the sensing coil can't pick up the ac field in the power line. A Rogowski coil has an air core and consists of a coiled piece of wire that wraps around the power line. Unlike an iron core, the air core doesn't saturate in the presence of a large permanent magnet. However, it's susceptible to other tampering methods, such as the presence of a large inductive field that couples into the coil and over-

AT A GLANCE

- Implementing the Smart Grid requires utility meters with electronic intelligence, tamper-proof electronics, and backup power.
- Magnetic and inductive fields do not affect shunt-based current sensors, as they do current transformers and Rogowski coils.
- Current transformers and Rogowski coils are inherently isolated sensors.
- Backup power sources allow power meters to record and transmit power-outage data when ac power is unavailable.

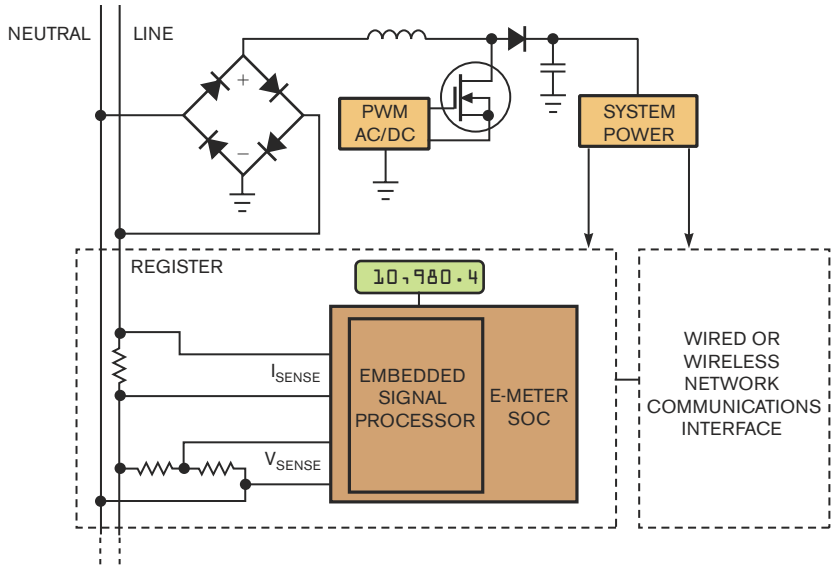

Figure 1 Smart power meters comprise a microcontroller with onboard ADC and DAC, a sensing component for both voltage and current, an ac/dc-power converter, battery backup, and wireless or wired communication capability.

whelms the ac current the coil is meant to sense.

Hall-effect sensors rely on a semiconductor device to sense the magnetic field caused by the alternating line current. But their readings can vary with temperature and are not always linear over a wide range of current. This problem is more significant in the US market, in which meters are rated as high as 200A, than in, say, India, where meters measure 20 or 40A. "Linearity becomes important in a market like the United States," says Kourosh Boutorabi, Teridian's vice president and general manager of the meter-products-business unit. "The requirement by utilities is for meters to have 0.2% error. Tolerances in the rest of the world are closer to 1% error. If you're consuming more power, then more loss in measuring is more important, and accuracy in measuring is more important."

Hall-effect sensors have advantages, too, he says. "Although they are not as accurate as [current transformers], they are cheaper." A Hall sensor can be pushed against [the power line] with no physical interconnection." With a current transformer, you have to manually assemble the power line and the sensing coil.

Most power meters worldwide are single-phase and use a simple shunt resistor as a current-sensing element. Cathal Sheehan, product-marketing manager for Bourns' resistive-products division, characterizes shunts as simple, inexpensive, and unaffected by the magnetic and inductive fields that befuddle magnetic and inductive sensors.

Mark Strzegowski, energy-metering-products-marketing engineer at Analog Devices, agrees that shunts provide no isolation between multiple phases, so you need to provide the isolation elsewhere. The company's approach is to use a shunt resistor with an isolating planar transformer it bases on the company's iCoupler technology for the isolating component: The iCoupler and shunt resistor combined are still cheaper than the cost of a current transformer or Rogowski coil, and they still preserve measurement linearity. "One of the things important to consider in selecting a current-sensing technology is the performance that the customer is looking for," says Strzegowski. "There has been a trend in the market toward wider dynamic ranges and also adding more measurements. You need to accurately measure 100A current all the way down to 100-mA current, with the same level of accuracy, since 0.1% is a typical accuracy spec."

USB in the FAST LANE

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High Speed USB Interface ICs

FEATURES

FT2232H (Dual High Speed USB to Multipurpose UART/ FIFO IC) has 4k bytes Tx and Rx data buffers per interface.

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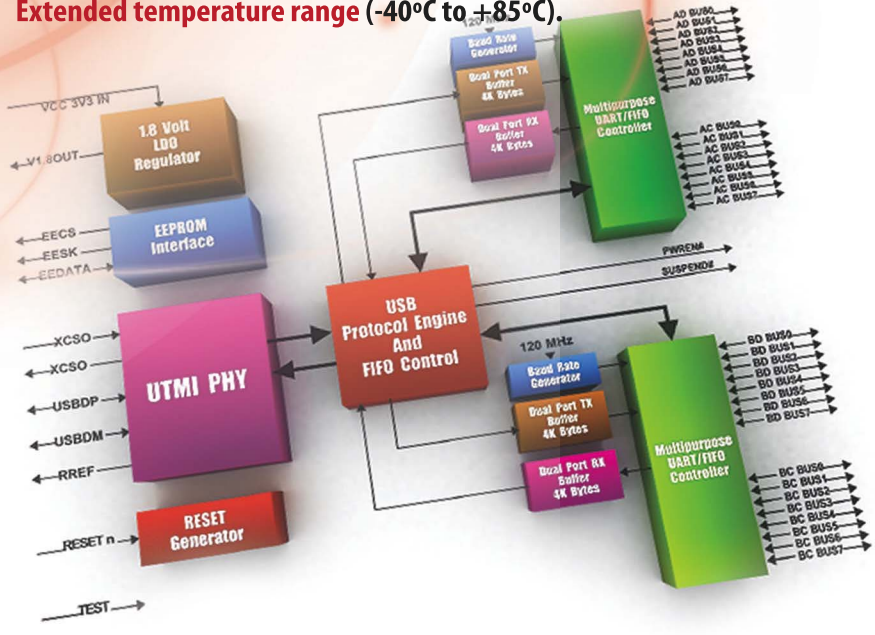

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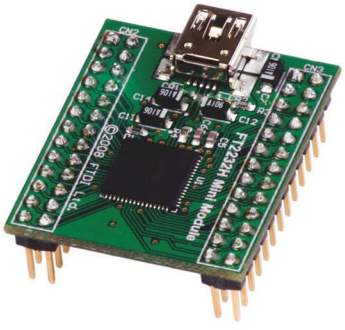
FT2232HQ

FT2232H Mini Module



FT4232HL

FT4232HQ

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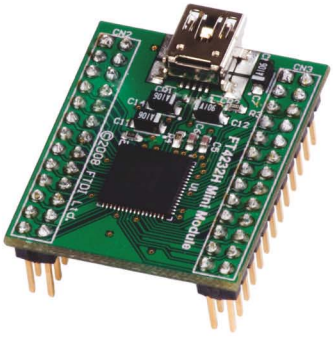

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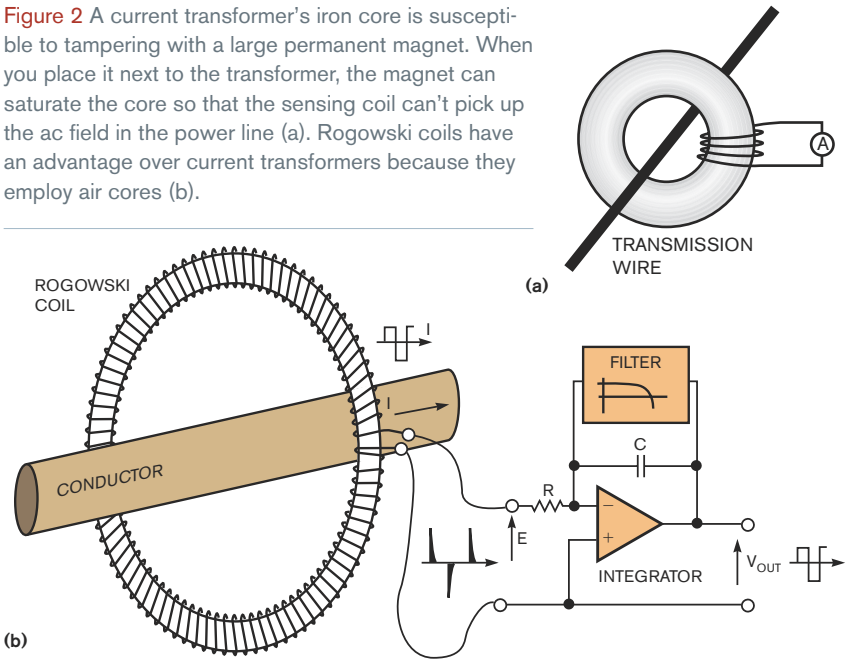
Figure 2 A current transformer's iron core is susceptible to tampering with a large permanent magnet. When you place it next to the transformer, the magnet can saturate the core so that the sensing coil can't pick up the ac field in the power line (a). Rogowski coils have an advantage over current transformers because they employ air cores (b).



Shunts have inherent problems with heating: Although their response is fairly linear, they can't handle some of the largest loads because of their self-heating effect. Likewise, current transformers typically have a small phase distortion that requires compensation, especially when applications require more sophisticated measurements, such as reactive- and harmonic-energy measurements. In general, single-phase power-distribution meters have shunt resistors for sensors, and three-phase meters have current transformers.

Silvestro Fimiani, product-marketing manager at Power Integrations, argues that, in addition to its being tamperproof, efficiency in a power meter is important, especially because there is the potential in the near future to install or replace more than 100 million power meters worldwide. "Over the life of the meter, you can waste as much as $20 in energy costs due to inefficient power usage in a meter," he says. "This [amount] can be as great as the cost of the meter." Fimiani may be a relatively lonely voice in the wilderness of smart meters calling out for power efficiency: Few other vendors are concerned with meter efficiency, possibly because the purchaser of meters, usually a utility, is not the entity that pays for the meter's power consumption. That cost is invisible but passes on to the consumer.

The components in a power meter should consume little power not only for the sake of cost savings and efficiency, but also to make sure that the meter operates efficiently when battery-powered. It's strange to think of a power meter's relying on battery power, but smart meters must be able to continue to operate even when there is a power outage.

The importance of battery backup in power meters depends on the region. In the United States, for example, if the power is down, there's nothing to measure, so there's little need to have the meter awake. Strzegowski of Analog Devices points out that, in India, however, some specifications require that there must be two batteries in the system. One powers meter reading and information storage for 24 or 48 hours and keeps the display alive. The other retains the meter information for as long as two years to prevent meter tampering. It removes the meter from the power line so that there is no voltage available to the meter electronics, but power is still flowing in the line.

Battery backup for power meters is often in the form of a lithium-thionyl battery, which has a self-discharge rate in the nanoamp region and a shelf life that exceeds 10 years. Tadiran is the largest manufacturer of these batteries in the United States. The battery alone is enough to back up data in the meter but

not to burst data out in a wireless communication. One approach is to use the battery to trickle-charge a supercapacitor. Pierre Mars, vice president of applications engineering at supercapacitor manufacturer Cap-xx, explains how government regulations affect the meters: "Even though the meter is connected to the mains and there is abundant power, the meter cannot use it to transmit data," he says. "One example is where I live in Australia, where the rules are [that] the meter cannot draw more than 2W of the user's power, so they need to use a [supercapacitor] to provide the burst power for GSM [global-system-for-mobile] communications transmission, which requires up to 6W for 0.6-msec bursts, with average power less than 0.75W." Mars notes that, if the government had written the rules in terms of energy used, rather than limiting peak power drawn, there would have been no problem.

In addition, supercapacitors provide adequate transmitting power for "last-gasp" transmissions, in which, in the event of a power failure, the supercapacitor backs up power to enable a transmission, alerting the meter that the power has failed.

Worldwide, power lost to tampered meters varies widely by region: The United States probably loses less than 4% to tampering, whereas India reports losses of greater than 10%, and losses in some Latin American countries can reach 20%. The search for a tamper-proof power meter is another reason to move toward smart power meters. One of the simplest and most common ways

GOOGLING YOUR POWER STATS

There is a truism in managing resources: You can't improve anything you can't measure. Google.org, the philanthropic side of Google, says, "We believe that everyone deserves access to their energy information to make smarter choices about energy use." So, Google is developing software that allows everyone to display their home power usage right on the Google home page (Reference A, Figure A).

The only catch is that the Google PowerMeter depends on the user's having a smart power meter. Currently, there are about 40 million smart power meters worldwide, but power utilities are planning to add 100 million more within a few years.

REFERENCE

A Power to the People, http://googleblog.blogspot.com/2009/02/power-to-people.html.

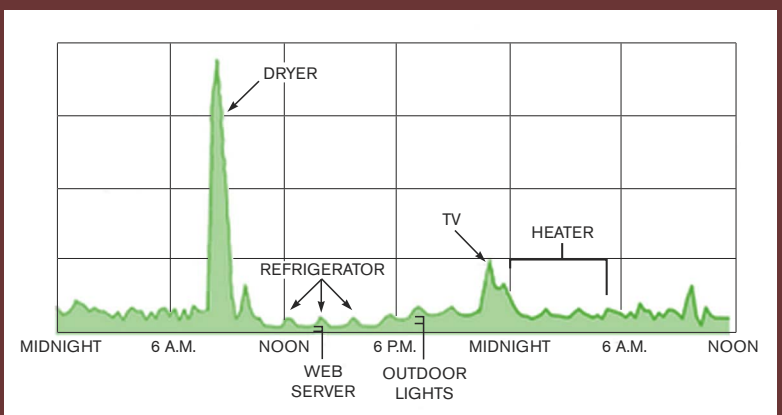


Figure A Google's PowerMeter software, currently in prototype, will receive information from utility smart meters and provide that information to homeowners on the Google home page. The information includes total energy consumption and energy consumption by time of day.

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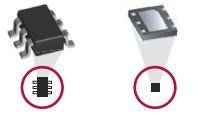

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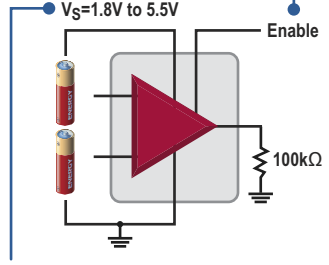

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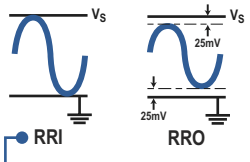

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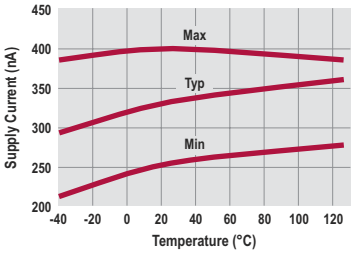

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to tamper with a power meter is through the sensor.

Why are antitampering methods important in the United States? At increasingly high electricity rates, a 4% loss is enough to get the utilities' attention. But, even more important, stolen power is the most common power source for illegal marijuana "grow houses." The power bill for such houses in urban areas can easily hit $10,000 a month, and stealing power from nearby power lines is a convenient way to get it. Neither nearby residents nor utilities are in favor of grow houses, so using smart meters is potentially an effective way to curb the activity. However, any activity that implies that a large organization, such as the government or a utility, is monitoring personal activities is a concern to some people (see **sidebar** "Googling your power stats.")

The rising cost of power has made fine-tuning of power metering for nonutility applications, too. Dave Heacock, senior vice president of TI's high-volume analog and logic business, says that server farms sometimes ask their front-end ac/dc-power-supply vendors to include power metering so that the farms can charge their customers according to their usage: The power they use at peak usage time will be subject to a higher rate. "Users [will] start to think, 'I'm going to do all my credit-card transactions at midnight when power costs less,'" Heacock says.

Tolerances for such an application will probably not be as tight as for a utility power meter: Heacock suggests representative tolerances for such metering devices are 2% for loads greater than 20% of full load, dropping down to 5% accuracy at 5% of full load. The reason for the relatively loose tolerance, he explains, is they don't want to add appreciably to the cost of the solution. EDN

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THE EDA TECHNOLOGY LEADER

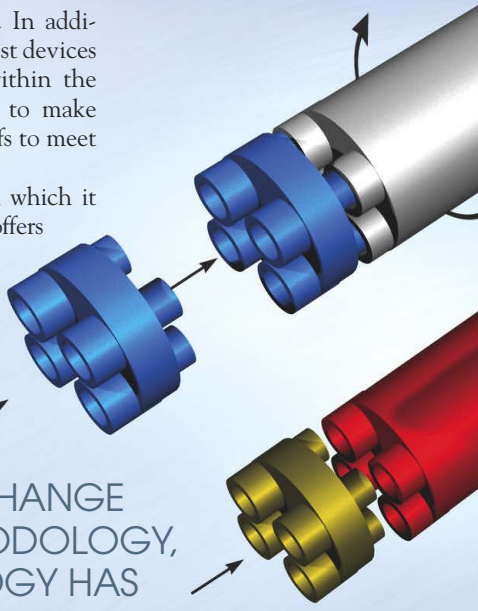
BY WARREN WEBB • TECHNICAL EDITOR

FPGAs RESHAPE EMBEDDED

As the economic slowdown takes its toll on development budgets, embedded-system designers are turning to FPGA (field-programmable-gate-array) technology to shorten design cycles, combat obsolescence, and simplify product updates. By taking advantage of a huge and growing arsenal of FPGA-development tools, reusable-logic elements, and off-the-shelf modules, designers can craft high-performance embedded systems that you can reconfigure for changes in requirements with a minimum impact on engineering and manufacturing. Traditionally, board designers have used these devices to interconnect system components, but the latest high-density products can also replace the processors, memory, custom logic, and many of the peripherals in a typical embedded project. Although it has the potential to transform embedded architecture, designers should analyze the performance, power, and cost limitations to determine where FPGA technology fits.

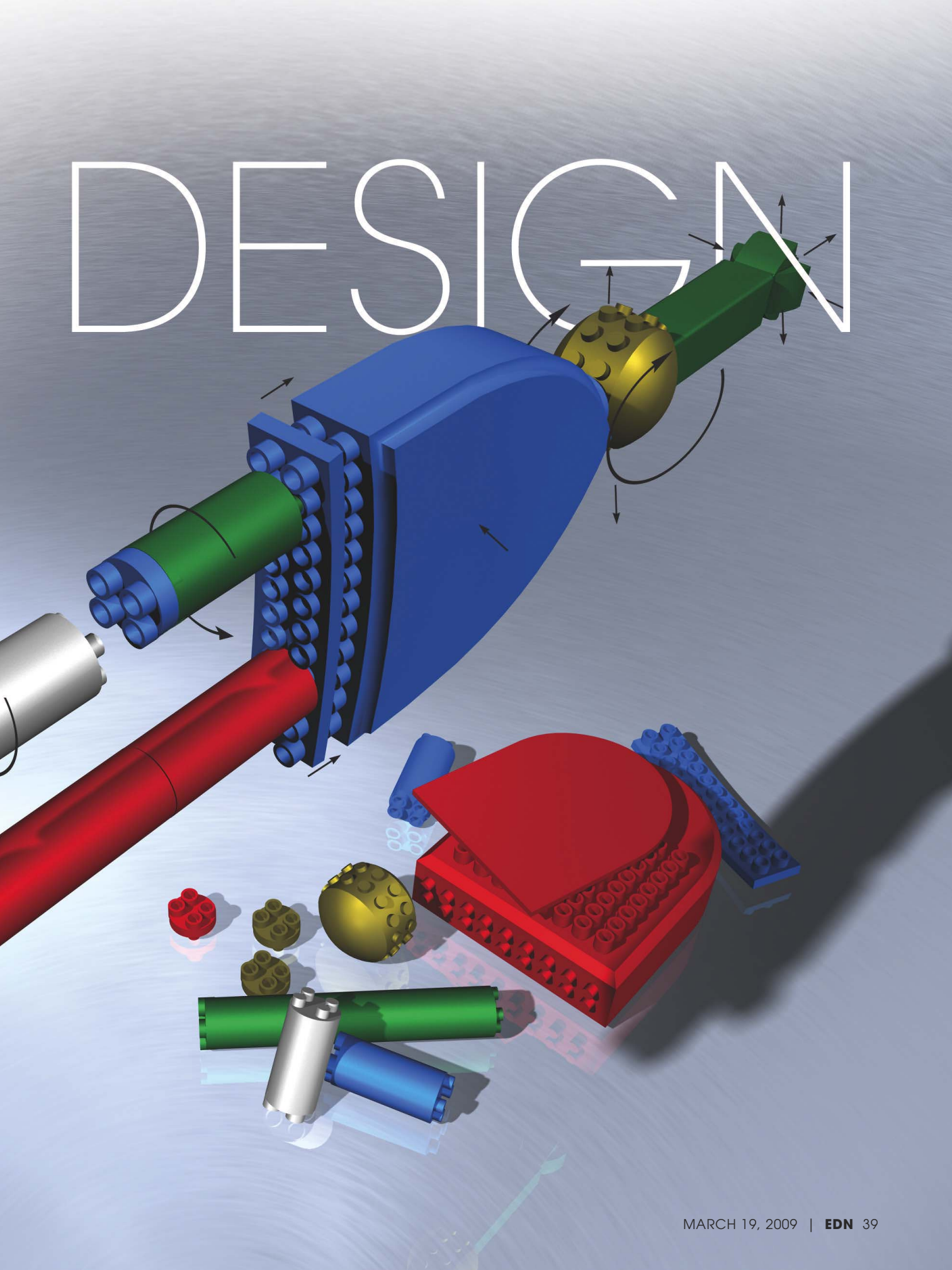
With roots in programmable-logic arrays from the 1970s, FPGA technology has developed into a thriving market with leaders Xilinx and Altera joining more specialized vendors such as Actel, Cypress, and Lattice. Although the exact makeup is different for each FPGA vendor, the basic FPGA architecture consists of arrays of logic blocks with electrically programmable interconnections that the user or designer can configure after manufacturing. Early devices contained the equivalent of a few thousand gates, but today's number has grown into the millions. This interconnection flexibility allows designers to create hardware functions that exactly match the needs of a specific embedded application. In addition to the logic blocks, the latest devices embed dedicated processors within the silicon, allowing the designer to make hardware and software trade-offs to meet performance requirements.

In embedded applications in which it is a match, FPGA technology offers developers multiple advantages over discrete or custom-logic implementations. Most experienced designers cite shorter



ALTHOUGH ITS USE REQUIRES A SIGNIFICANT CHANGE IN DESIGN METHODOLOGY, FPGA TECHNOLOGY HAS BECOME A VALUABLE WEAPON IN THE EMBEDDED-SYSTEM DEVELOPER'S ARSENAL.

DESIGN



development schedules, lower nonrecurring costs, and the ability to incorporate changes after production as their primary reasons for incorporating FPGAs. In high-performance applications, designers can create multiple parallel-computing structures that can outperform dedicated processors. One of the often-mentioned disadvantages of FPGA technology is the additional power required compared with a general-purpose processor or custom ASIC. Similarly, because of the resistance of multiple pass transistors and connection paths, FPGA-based products are also slower than comparable conventional designs. Although it does not take the development time of other approaches into account, the recurring cost of FPGA technology is higher than that of conventional or custom circuitry.

FPGA vendors use multiple techniques for programming the interconnections and logic blocks. For example, the antifuse-silicon structure creates a low-resistance link when you apply a high voltage across its terminals. Advantages include low series resistance and low parasitic capacitance, but the main disadvantage is that an antifuse-based FPGA is a write-once device and therefore not reconfigurable. Static RAM cells, the most common programming technique, enable or disable pass transistors to program FPGA topology. Although you need several transistors to implement a memory cell, SRAMs provide fast reprogrammability, and you can implement them in conventional silicon-CMOS technology. SRAM-based FPGAs also require an external boot device to set the memory on power-up. You can also use EPROM, EEPROM, and flash-memory technologies to program FPGAs, with the advantages of reprogrammability and elimination of the external boot-up device.

Manufacturers have also created multiple methods to describe and program FPGA circuitry. The most common approach is to use an HDL (hardware-description language), such as Verilog or VHDL (very-high-speed-integrated-circuit HDL), to describe the functions and topology of a design. Once you have defined the architecture, you can use additional tools to implement the structure on a given FPGA. This process includes power and configuration optimization followed by hardware partitioning, placement, and interconnection routing. The final stage is to load the design onto the target FPGA for testing in the actual hardware environment.

As FPGA functions grow in complexity and density, designers have devised ways to exchange modular blocks of HDL code that others can incorporate into their products. These functional blocks, commonly referred to as IP (intellectual-property) cores, allow manufacturers to reuse circuit elements from previous designs or simply purchase functions from an outside source. Examples of IP cores include UARTs, Ethernet interfaces, codecs, and microcontrollers. Manufacturers physically implement hard IP cores directly onto the silicon of a FPGA and provide soft cores as HDL code that is portable across multiple devices. IP cores are available directly from FPGA vendors and third-party suppliers or as freely available open-source HDL code from sources such as Open Cores. Commercial IP is usually

AT A GLANCE

- FPGA (field-programmable-gate-array) architecture lets you reconfigure embedded systems for changes in requirements with a minimum impact on engineering and manufacturing.
- FPGA designs combine multiple components into a single package to reduce component count, board size, and manufacturing complexity.
- Drop-in IP (intellectual-property) cores from device vendors, third-party suppliers, and the open-source community ease FPGA setup.
- Designers segment FPGA-based signal-processing algorithms into parallel-computing structures to boost performance.
- Tools to specify FPGA configurations range from low-level HDLs (hardware-description languages) to high-level graphical-design environments.

Figure 1 The Xilinx embedded development kit includes tools and a prototyping board, on which users can edit, simulate, compile, and test Virtex-5 designs.

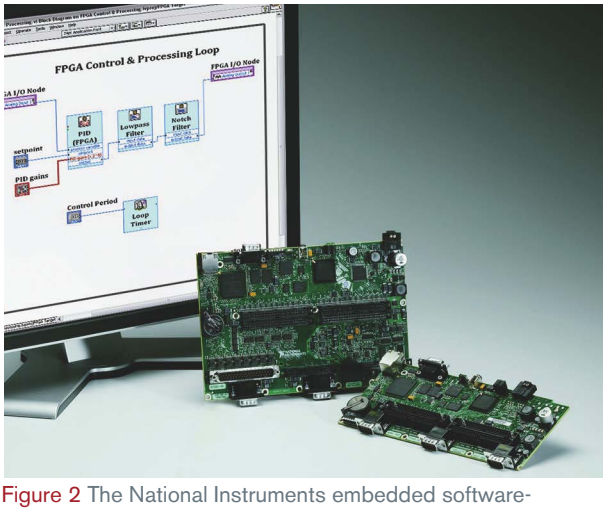


Figure 2 The National Instruments embedded software-evaluation tool kit allows users to create, compile, and run FPGA applications from a graphical block diagram.

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34410A	6 ½	0.0030%	10,000 / sec	2.6 ms	GPIB, USB, LAN (LXI)
34411A/ L4411A	6 ½	0.0030%	50,000 / sec	2.6 ms	GPIB, USB, LAN (LXI)
34420A	7 ½	0.0030%	250 / sec	.02 sec	GPIB, RS-232
3458A	8 ½	0.0008%	100,000 / sec	3.0 ms	GPIB

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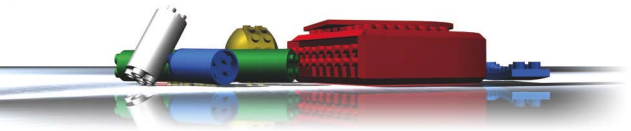


fee-based and includes documentation, verification tools, and support.

Design security and loss of IP can be a major concern for some FPGA developers. In some cases, especially those SRAM designs that store configuration data externally and transfer it to the FPGA on power-up, IP information is vulnerable. To combat IP loss, FPGA vendors use nonvolatile programming techniques along with embedded serial numbers to trace counterfeit products. Altera offers another technique for securing a design and lowering the recurring cost of a device. The company's HardCopy ASIC has features equivalent to those of the corresponding Altera Stratix series FPGA and offers resources comparable to those of the FPGA but with smaller die and lower power requirements. The final HardCopy ASIC is a pin-for-pin replacement of the FPGA prototype, allowing it to retain the system board and software between prototyping trials and the final production device. You can realize additional overall board savings by using the HardCopy ASIC for production because it requires no boot device.

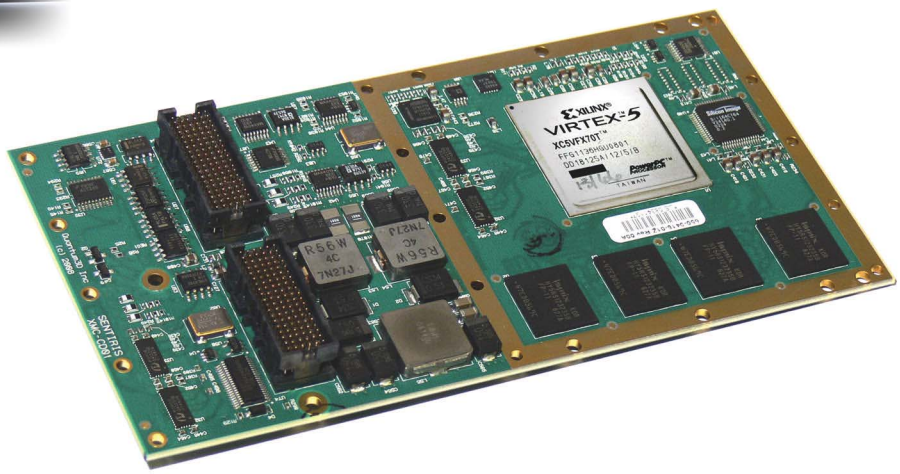


Figure 3 The Sentiris AV1 PCI express mezzanine card from Quantum3D fights obsolescence by incorporating an FPGA-based video- and graphics-processing core.

All FPGA vendors offer a tool set that combines programming tools with IP verified to work with their devices. For example, the EDK (embedded development kit), Virtex-5 FX70T edition from Xilinx provides an ML507 development board, the Platform Studio embedded tool suite, and ISE (integrated software environment) supporting the PowerPC 440 hard and MicroBlaze soft processors (**Figure 1**). The kit features an integrated development environment, multiple software tools, configuration wizards, and IP targeting embedded design. Users can input a circuit in the schematic editor, simulate the timing behavior of the

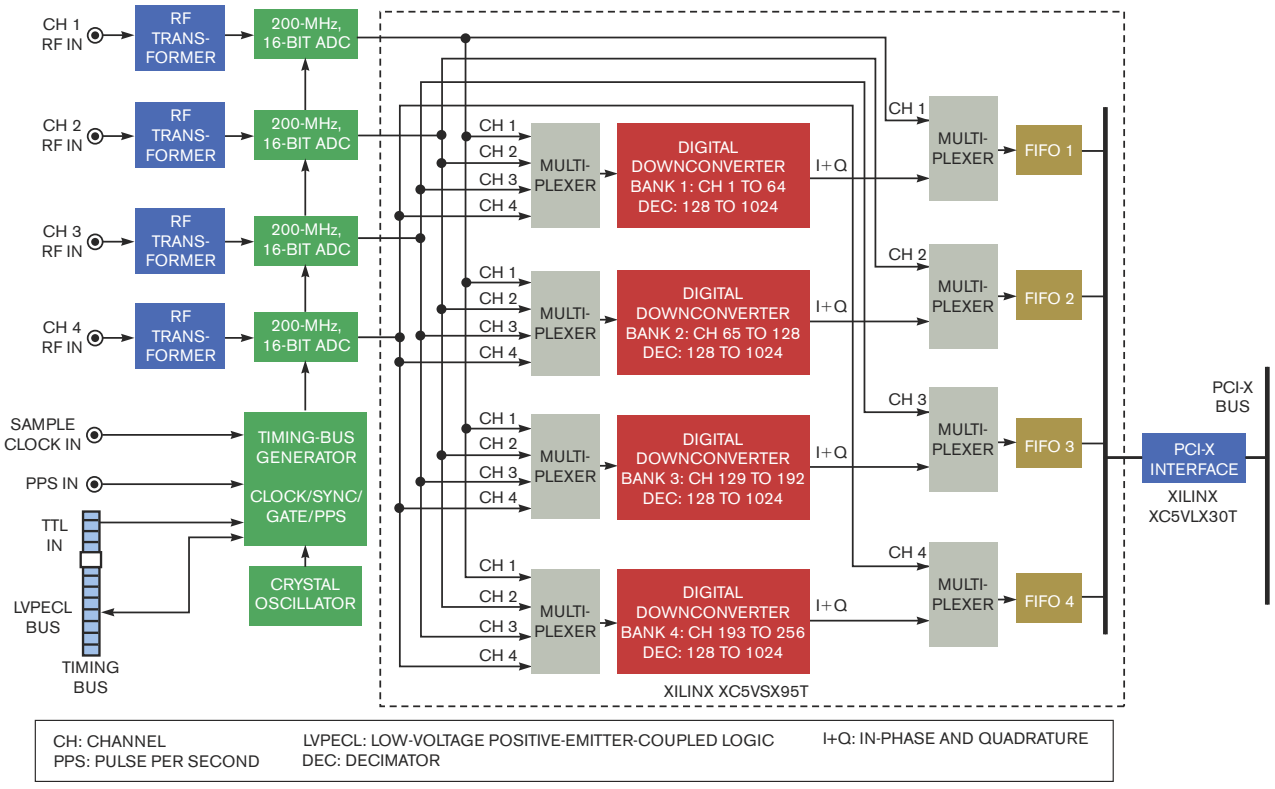
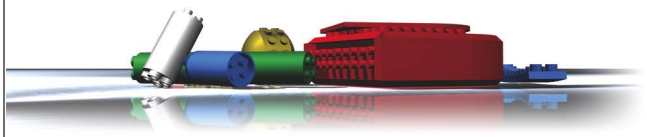


Figure 4 The Model 7151 software-radio module from Pentek features a proprietary FPGA-IP core that delivers 256 channels of digital downconversion.

circuit, compile it for a Virtex-5 FPGA, and test the design on the ML507 prototyping board. You can buy the Virtex-5 FX70T EDK online for $2595.

GRAPHICAL DESIGN

FPGA-development tools are also available from third-party vendors and embedded-board manufacturers. For example, National Instruments recently introduced an FPGA-based, single-board RIO (reconfigurable-I/O) module suitable for embedded applications along with an evaluation kit demonstrating programming techniques using its LabView graphical-design software. The new modules combine a real-time embedded processor and a reconfigurable FPGA plus analog and digital I/O on a single 8.2×5.6-in. PCB (printed-circuit board). The modules feature a 266- or 400-MHz Freescale MPC5200 processor, the Wind River VxWorks real-time operating system, and a Xilinx Spartan-3 FPGA. The onboard analog and digital I/O connects directly to the FPGA to provide low-level customization of timing and I/O signal processing. Prices for the single-board RIO de-



WITH ITS SUPERIOR PARALLEL-PROCESSING CAPABILITIES, FPGA TECHNOLOGY MAKES SENSE FOR HIGH-PERFORMANCE, MULTICHANNEL APPLICATIONS.

vices start at $1000 (100 or more).

In support of the single-board RIO, National Instruments also introduced the embedded software-evaluation tool kit to evaluate the LabView Real-Time and LabView FPGA programming experience for embedded applications. The kit includes extended evaluation software, an NI single-board RIO evaluation device, a daughterboard for I/O interfacing, a power supply, cables, a step-by-step tutorial, and several ready-to-run examples of common embedded tasks implemented in LabView (**Figure 2**). The kit includes several exercises to create, compile, and run FPGA applications by building and fine-tuning a graphical block diagram in LabView. A 90-day version of the LabView embedded platform-evaluation kit costs $999.

A growing number of commercial-board-manufacturing companies are exploiting FPGA technology to satisfy complex design requirements and allow for future changes. For example, Quantum3D promises obsolescence-proof hardware in safety- and security-critical applications, such as primary flight instrumentation and MLS (multilevel-security) systems, with a new Sentiris AV1 PCI XMC (express mezzanine card) (**Figure 3**). The vendor incorporates an FPGA-based video- and graphics-processing core instead of the traditional dedicated GPUs (graphics-processing units). Although originally designed for applications such as flight-certified image generation, Sentiris AV1 is also applicable for other uses, such as real-time imaging for medical applications. The product's video- and graphics-processing capabilities with analog and HD-SDI (high-definition serial-digital interface)-video outputs enable 3-D graphics in cockpits and mission-critical applications. Sentiris AV1 offers 512 Mbytes of ECC-protected DDR2 memory, dual HD-SDI outputs, and eight lanes of PCIe (peripheral-component-interconnect express). Prices for the Sentiris AV1 start at $9980.

With its superior parallel-processing capabilities, FPGA technology makes sense for high-performance, multichannel applications, such as software radio, data acquisition, and digital-signal processing. For example, Pentek recently introduced the Model 7151 high-resolution software-radio module for GSM (global-system-for-mobile)-communications cell-phone-monitoring and signal-intelligence applications (**Figure 4**). Four 200-MHz, 16-bit ADCs feed a proprietary FPGA-IP core that delivers 256 channels of DDC (digital downconversion). You can configure each bank of 64 DDC channels for a unique output-signal bandwidth to accommodate applications requiring mixed signal types or multiple modulation schemes. You can independently source each DDC bank from any of the four ADCs, which are typically assigned to specific antennas. The Model 7151 allows the user to simultaneously capture hundreds of signals spanning a range of modulation types, signal bandwidths, and antenna sources. Pentek offers the ReadyFlow board-support package to provide developers with a complete library of hardware initialization, control, and application functions for Linux, Windows, or

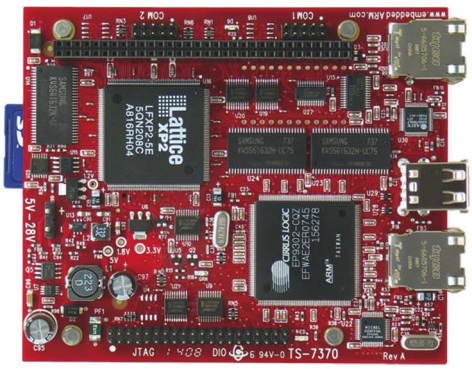


Figure 5 TS-7370 from Technologic Systems includes a user-programmable FPGA allowing you to create a custom interface to most color TFT-LCD panels.

VxWorks operating systems. The Model 7151 PMC (PCI-mezzanine-card)-module version is available for $14,500.

EMBEDDED STANDARDS

Standards organizations specializing in embedded systems are also adopting a new design specification based on FPGA hardware. For example, the recently ratified VITA (VMEbus International Trade Association) 57.1 FMC (FPGA-mezzanine-card) standard makes it easier for developers to integrate FPGAs into embedded-system designs. The specification defines I/O devices that reside on an industry-standard mezzanine card that you attach to FPGAs that reside on a baseboard. The FPGAs directly control the devices. The FMC approach allows you to reuse a single FPGA design on multiple projects by simply replacing the I/O section. An FMC module is about half the size of a standard PMC module. Vmetro, a Curtiss-Wright company, introduced one of the first I/O modules, basing it on the FMC standard. The ADC510, available in air- and conduction-cooled, rugged versions, integrates two 12-bit, 500-MHz ADC chips for use in digital-signal-processing applications, such as radar, signal intelligence, and electronic countermeasures.

Low-cost, commercial-off-the-shelf embedded modules are also adopting FPGA technology to give designers flexibility in custom applications. For example, the TS-7370 from Technologic Systems is a PC/104-form-factor, LCD-ready single-board computer that the company based on the Cirrus EP9302 200-MHz ARM9 CPU and a user-programmable Lattice XP2 FPGA (**Figure 5**). The company designated the product LCD-ready because the FPGA connects to a dedicated RAM frame buffer, allowing users to create a custom video core on the FPGA to provide an interface to most color TFT (thin-film-transistor)-LCD panels. Supporting multiple embedded-system applications, the TS-7370 peripheral interfaces include onboard RAM, 10/100-Mbps Ethernet, USB 2.0 host, serial ports, an SD (secure-digital)-card socket, ADC channels, digital-I/O lines, a temperature sensor, and a real-time clock. The TS-7370 runs Linux 2.6 out of the box and costs $149 (100).

As design teams adjust to reduced budgets and increased system complexity, FPGA devices and development tools have become major considerations in new embedded designs. FPGAs provide a way to create multiple system configurations with a single hardware design. The reconfigurable devices are especially valuable in high-speed, multichannel systems with performance requirements that are difficult to meet with traditional microprocessor-based architecture. Although the added recurring cost and power required for FPGA designs limit their application, they are a great choice for low- to medium-volume projects that will benefit from reduced risk, shorter design cycles, and minimized nonrecurring engineering. EDN

For more on re-engineering obsolete ICs with FPGAs, go to www.edn.com/article/CA6604712.

To read about how the universal-submodule concept cuts I/O-design costs and time to market, visit www.edn.com/article/CA6615159.

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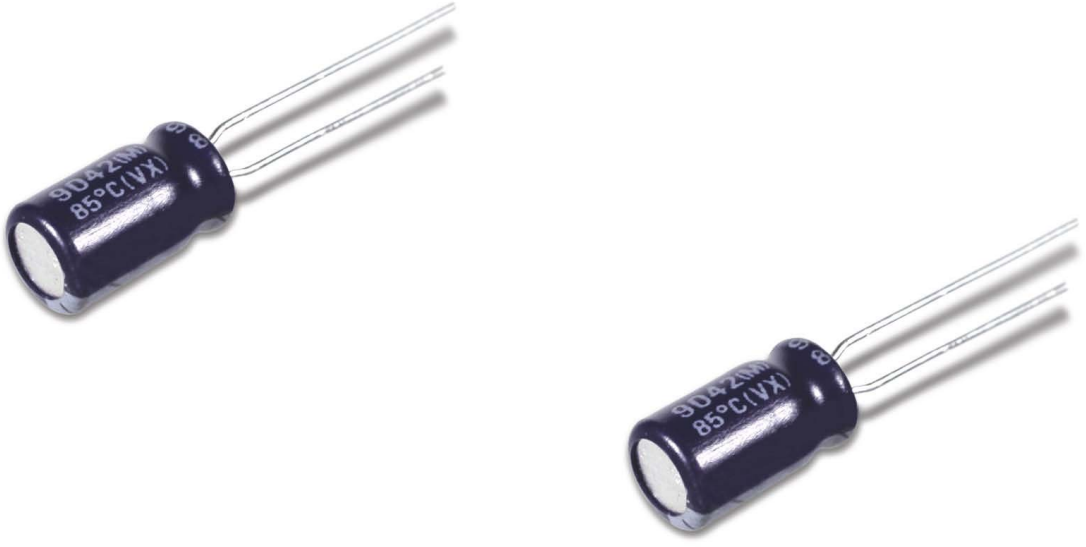

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Whatever happened to my dynamic range?

IF YOUR TESTING RESULTS DON'T CLOSELY APPROXIMATE THE SILICON VENDOR'S SPECIFICATION CLAIMS, QUESTION YOUR ASSUMPTIONS BEFORE CONCLUDING THAT YOUR SUPPLIER IS INFLATING THE NUMBERS.

Recently, a customer who had implemented a design using a high-performance, 120-dB-dynamic-range ADC/DAC pair complained that he was getting only 113-dB performance. At first glance, this issue appears serious, but a relatively simple explanation exists: The dynamic range for audio converters is an SNR (signal-to-noise ratio) that you measure over a specified bandwidth with a signal that is −60 dBFS (decibels full-scale). You add 60 dB to the resulting measurement to reference the measurement to digital full-scale. The intent is to provide the specification for a full-scale SNR that excludes distortion components. The assumption is that the distortion components are negligible at this signal level and therefore do not require any processing to remove them.

The AES (Audio Engineering Society, www.aes.org), the IEC (International Electrotechnical Commission, www.iec.ch), and others publish this technique in most of their audio-testing standards. The specifications also include a requirement for a weighting filter that reflects the frequency sensitivity of the human ear over the 20-Hz to 20-kHz audio bandwidth. In summary, the goal of the audio dynamic range is to provide an easily measured full-scale SNR specification that reflects the sensitivity of human hearing.

Measuring audio-system dynamic range is a relatively simple matter, thanks to the plethora of advanced test and measurement tools available from Audio Precision (www.ap.com), Rohde & Schwarz (www.rohde-schwarz.com), and other companies. However, several factors, including measurement bandwidth, sample rate, and weighting filters, have a direct impact on the measurement. A typical dynamic-range specification is an A-weighted, 120-dB figure that you measure from 10 Hz to 20 kHz at a 48-kHz sample rate. You must take into account each of these measurement parameters when comparing measured results with ADCs and DACs.

SAMPLE RATE AND MEASUREMENT BANDWIDTH

It is enlightening to review the relationship between SNR, measurement bandwidth, and sample rate for audio ADCs. One of the fundamental characteristics of quantizing an analog signal is that you can divide all of the signal energy at frequencies above the sample rate, F_S, by two to alias into the frequency region between dc and $F_S/2$. This signal energy includes noise from the analog-signal source, noise from the sampling networks, and quantization noise. Essentially, all signal energy exists between dc and $F_S/2$ within the digital domain. A subtle but important nuance therefore exists regarding audio measurements in which the standard 20-kHz upper-bandlimiting frequency does not extend to $F_S/2$.

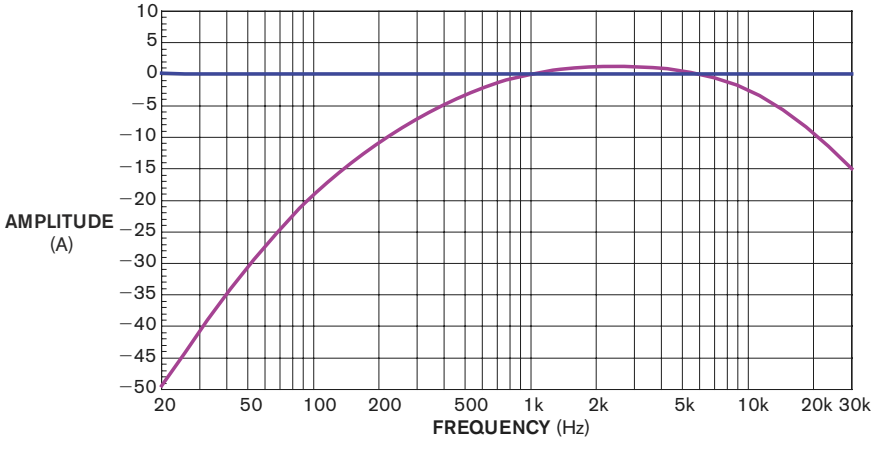

Figure 1 The frequency response of an A-weighting filter (purple) stacks up against a reference unweighted (blue) frequency-response plot (source equipment: Audio Precision).

For example, 48 kHz is a common audio-sample rate, in which the noise is distributed between dc and 24 kHz. However, with the measurement bandwidth limited to 20 kHz, the measurement therefore includes only 83% of the total bandwidth. It is a relatively simple matter to calculate the difference in the SNR measurements as a function of measurement bandwidth: $10\log(BW_1/BW_2)$, where BW is the bandwidth. This **equation** is valid only for white noise—that is, noise with a signal having equal power per unit of bandwidth. For example, at a 48-kHz sample rate, where $F_S/2$ is 24 kHz, the difference in the SNR measurement is nearly 0.8 dB when you bandlimit it to 20 kHz. However, with the same 20-kHz, bandlimited

measurement at a 44.1-kHz sample rate, the measurement includes almost 91% of the total noise. The difference in the SNR at 44.1 kHz is only 0.424 dB. Notice that a difference of 0.37 dB exists in the 20-kHz, bandlimited measurements between the 48- and 44.1-kHz sample rates.

So, ADC SNR with a bandwidth of dc to $F_S/2$ is the same for both the 44.1- and the 48-kHz sample rates. However, this equivalency no longer holds true when the measurement bandwidth is 20 kHz. This discrepancy should also give some insight about why audio-converter manufacturers typically specify performance at a 48-kHz rather than a 44.1-kHz sample rate.

WEIGHTING FILTERS AND ADCs

Dynamic-range specifications include a weighting filter that allows the measurement to correlate to human hearing. Although audio-testing standards mention several weighting filters, audio-converter manufacturers most commonly use the ANSI (American National Standards Institute, www.ansi.org) A-weighting filter (**Figure 1**). One of the more common measurement differences when comparing measured results with data-sheet specifications is to exclude the A-weighting filter. When you bandlimit the measurement to 20 kHz, there is a 2.5-dB difference between the weighted and the unweighted results, assuming that the noise is uniformly distributed at 20 kHz. Without the A-weighting filter, the 120-dB converter specification degraded to 117.5 dB. It is relatively easy to demonstrate these effects using the evaluation board for the Cirrus Logic (www.cirrus.com) CS5381 ADC and the Audio Precision System 2 (**Table 1**). Notice that these measurement results differ by as much as 3.3 dB based on sample rate, measurement bandwidth, and weighting.

TABLE 1 CS5381 PERFORMANCE AT 44.1 AND 48 kHz

Measurement configuration	48-kHz sample rate	44.1-kHz sample rate
20-kHz bandwidth	117.5	117.2
20 kHz A-weighted	120	119.6
$F_S/2$	116.7	116.7
$F_S/2$ A-weighted	119.7	119.5

DAC DYNAMIC RANGE

The measurement issues for ADCs also apply to DACs, with the additional complication that the measurement is within the analog domain in which noise extends well beyond $F_S/2$. This broadband noise combines with the multiple measurement-bandlimiting options available in the measurement equipment to yield a multitude of valid measurements that do not accurately reflect converter-specification parameters. Recall that you can calculate the difference in a noise measurement as a function of bandwidth assuming that the noise is white.

To further complicate matters, highly oversampled delta-sigma DACs generate noise with a density that increases as the frequency increases. The delta-sigma-shaped out-of-band noise does not fit the definition of *white noise*. As a result, surprisingly large differences in dynamic-range measurements can occur as a function of measurement bandwidth. It is relatively easy to demonstrate these effects using, for example, the evaluation board for the Cirrus Logic CS4398 DAC and the Audio Precision System 2 (**Table 2**). These measurements, which came from a properly operating evaluation board meeting data-sheet specifications, differ by as much as 48 dB based on sample rate, measurement bandwidth, and weighting.

TABLE 2 CS4398 PERFORMANCE AT 44.1 AND 48 kHz

Measurement configuration	48-kHz sample rate	44.1-kHz sample rate
22 kHz	117.6	117.5
22 kHz A-weighted	120.5	120.4
30 kHz	116.4	116
30 kHz A-weighted	120.5	120.4
80 kHz	100.4	96.4
80 kHz A-weighted	120.4	120.1
500 kHz	73.5	72
500 kHz A-weighted	119.9	119.2
20 kHz Brickwall	118.2	118
20 kHz Brickwall A-weighted	NA	NA

COMBINED ADC AND DAC DYNAMIC RANGE

A commonly overlooked characteristic of an ADC-plus-DAC system is that each converter is an independent noise source. The following **equation** represents the combined noise: $[(N_{ADC})^2+(N_{DAC})^2]^{½}$, where the ADC noise is N_{ADC} and the DAC noise is N_{DAC}. The common misconception in this regard is that a system comprising equal-dynamic-range ADCs and DACs results in a combined specification equal to that of the individual converters. For example, a properly implemented and measured system with a 120-dB DAC and a 120-dB DAC yields a combined SNR specification of 117 dB. Again, it is relatively easy to demonstrate the possible outcomes using the Audio Precision System 2 and the evaluation boards for the CS5381 ADC and the CS4398 DAC (**Table 3**). Similar to the DAC measurements, these measurement results differ by as much as 45 dB based on sample rate, measurement bandwidth, and weighting.

REVISITING THE CUSTOMER'S COMPLAINT

Going back to the customer's original complaint, how do you determine the cause of the discrepancy? The first step is to understand which functional components are in the sig-

nal chain. I learned that the measured SNR was a combined ADC/DAC measurement between the analog input and the analog output. With that knowledge alone, I quickly located the 3 dB of the "missing" dynamic range: The combined performance measurement that the data sheet specifies is 117 dB. Continuing the discussion with the customer, I identified the configurations of sample rate, measurement bandwidth, and weighting filters. With this knowledge, I learned that the system operates at a 48-kHz sample rate, with a 22-kHz measurement bandwidth without the A-weighting filter. This configuration should result in a measurement of approximately 114.5 dB with properly implemented converters (**Table 3**). As if by magic, the customer and I found 5.5 dB of the missing dynamic range. Now, however, comes the hard part. What happened to that last decibel? EDN

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TABLE 3 CS5381-PLUS-CS4398 PERFORMANCE AT 44.1 AND 48 kHz

Measurement configuration	48-kHz sample rate	44.1-kHz sample rate
22 kHz	114.5	114.2
22 kHz A-weighted	117.2	116.9
30 kHz	113.6	113.3
30 kHz A-weighted	117.2	116.9
80 kHz	100.2	96.3
80 kHz A-weighted	117	116.7
500 kHz	73.5	72
500 kHz A-weighted	116.7	116.2
20 kHz Brickwall	114.9	114.7
20 kHz Brickwall A-weighted	NA	NA

AUTHOR'S BIOGRAPHY

Steve Green is a technical-marketing manager at Cirrus Logic. He has more than 30 years' experience in the audio industry, including more than 17 years with Crystal Semiconductor and (post-acquisition) Cirrus Logic as an applications engineer, applications manager, and technical-marketing engineer. Green is active within the Audio Engineering Society; he wrote several convention papers and served as an invited speaker at several AES section meetings around the United States and as a speaker for design tutorials at the AES convention related to the implementation of delta-sigma converters. Before joining Crystal Semiconductor and Cirrus Logic, he worked as a systems-design engineer in the professional-audio industry. Green earned a bachelor's degree in electrical engineering from the University of Texas—Austin.

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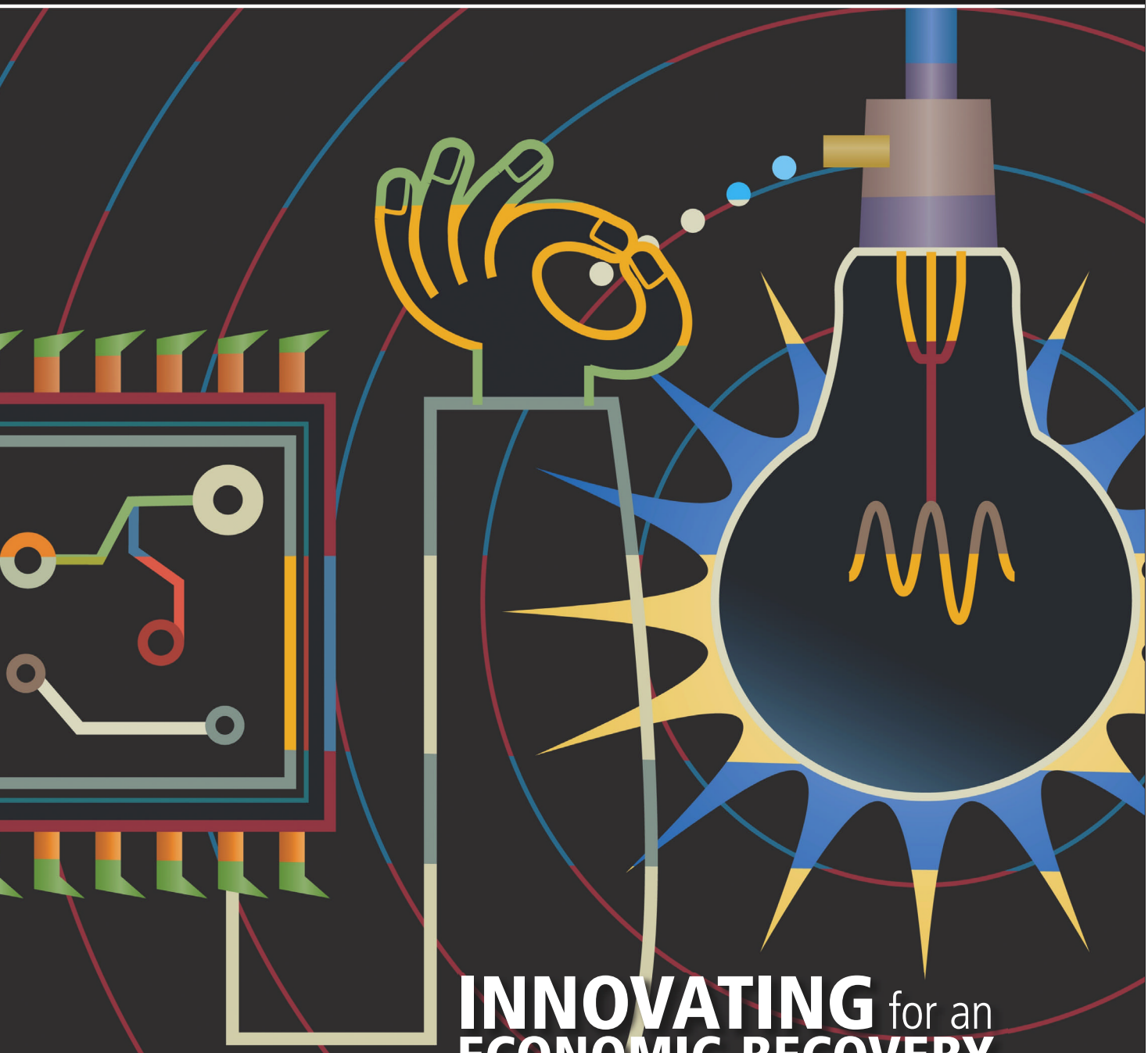

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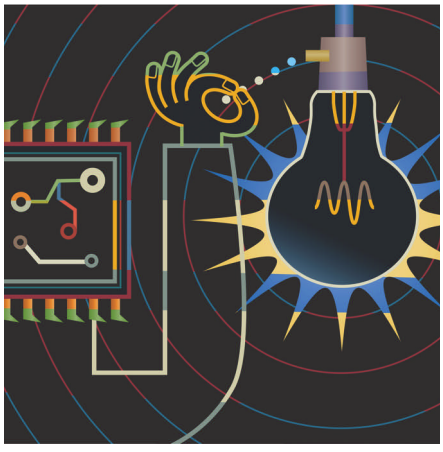

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INNOVATOR OF THE YEAR FINALISTS

As part of its ongoing commitment to recognizing and honoring excellence in electronics engineering, *EDN* recently requested nominations for its 19th annual Innovation Awards. Voting is complete, and the winners will be named March 30 during an eagerly awaited awards dinner in San Jose, CA. *EDN* editors sat down and spoke with one individual and three teams—the four finalists in the Innovator of the Year category—to gain insight into the thought processes behind the innovations.

FEATURES

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Altera | DESIGN TEAM

Bringing giant FPGAs to a new node

Altera Corp's design team for its 40-nm Stratix IV FPGA provides an example of the huge amount of work it takes to be the first to use a new process.

By Ron Wilson, *Executive Editor*

"This could work only because we both had the same goal: a successful FPGA launch."

MOLY CHIAN
Altera

Engaging with TSMC's (Taiwan Semiconductor Manufacturing Co's) 40-nm process-development effort toward the end of 2006, Altera had to simultaneously work with TSMC on process development, develop the FPGAs that the company would build using the process, create the IP (intellectual property), and design tools for the new chips.

This need for near-simultaneity led to a multitrack project organization. One substantial team at Altera worked with TSMC just on process development. Another team worked on the silicon design of the Stratix IV. Two additional teams worked on tool and IP development for the new FPGAs. "We chose to schedule our first tapeout of the design shortly after process qualification," says Moly Chian, Altera's vice president of technology development. "To achieve that [goal], all through the schedule the chip design and the process had to advance together."

Technological development

In 2006, when Altera first became involved with the 40-nm node, TSMC's process was barely more than a set of equipment choices and design goals. At that stage, the process models suggested only how a 40-nm transistor might look. From this early stage, however, Altera's and TSMC's work would have to converge. To do so, Chian explains, Altera and TSMC had to agree on a two-phase cooperative relationship: "target-driven process development." During the development, Altera would turn process data into device models, using these models to check against their FPGA design requirements and suggesting changes to TSMC.

"In the first phase," Chian says, "the models tracked the process development." During this time, the process

The San Jose, CA, portion of Altera's design team included (left to right) Neville Carvalho, Chong H. Lee, Jeff Watt, Srinivas Reddy, Shawn Wang, Bergen Hung, Peter McElheny, Andrew Leaver, CK Sung, Zunhang Yu Kasnavi, Chris Finan, Elvis Fu, Sergey Shumarayev, John Xie, Bill Liu, and Renxin Xia. Not pictured: Qi Xiang

was evolving rapidly, and the two teams would periodically take a snapshot of the process models, translate these into transistor models. This phase ended nearly as soon as TSMC and Altera could project trend lines for the process parameters, says Chian.

The two companies then moved into the second phase. "At this point, we knew enough about what the process could do and what we needed of it that we could define targets for the process," Chian continues. "Once we agreed on a set of targets, the work changed. Now, the process had to converge on the targets, rather than the models tracking the process."

This technique was a major excursion beyond the comfort zone for many at TSMC. The process engineers in Taiwan have a tradition of being conservative about their commitments until they have silicon in hand. With Altera's team, however, they agreed to commit to a set of targets that looked achievable but that they had not actually measured in silicon. "This could work only because we both had the same goal: a successful FPGA launch," Chian says.

Chip design

The chip design began with architectural exploration long before Altera and TMSC froze the transistor model. The basis of the early work was the internally developed FMT (FPGA-modeling tool). This system-level simulation environment allows architects to breadboard the characteristics of an FPGA architecture—the circuit and logic cell designs, interconnect-fabric details, power, and performance figures—and then examine the behavior of a complete FPGA with those characteristics. The result is a simulation of the FPGA product that the customer would see: the capacity, performance, power, compilation time, and so on, for real customer-IP blocks.

Thus, the FMT became not only the architects' primary tool for exploring chip-design alternatives, but also the primary way of understanding the impact of process, circuit-design, and design-tool choices on the end product. Reflecting the growing importance that design tools are assuming in the customer's view of an FPGA product, the architectural modeling started in the tools group, not in the chip-design area.

Early on, according to Altera's vice president for IC design, Richard Cliff, the architects made some rather conservative decisions based on marketing's requirements and results from the FMT. "We chose not to change either the logic cell design or the routing fabric from the 65-nm Stratix III," Cliff says. "This was primarily a time-to-market decision."

Once Altera and TSMC froze the process targets, the chip design could progress from architecture to design of specialized cells, synthesis of the major FPGA components, and test-chip builds. This workflow required teaming not just with TSMC, but with Altera's EDA partners, such as Synopsys. "We had to rely on internal tools early on," Cliff says. "The design exceeded the capacity of the commercial tools. We were seeing runtimes an order of magnitude greater than we had experienced for the previous generation of chips. So, we worked with TSMC and Synopsys to abstract the models and evaluate them faster and to use the tools in novel ways."

A key part of the chip-design effort was the creation of eight test chips during the course of the project. These chips ranged from small structures to help understand the process and define the targets to a complete transceiver channel to thoroughly verify the critical analog-transceiver design. Interestingly, one of the early test chips was a complete Stratix-III-class FPGA, which the designers automatically ported from its 65-nm database. This approach not only gave the team confidence with a full chip in the new process, but also highlighted the areas that would require more than just resynthesis with the new libraries.

The complete FPGA also gave TSMC a test vehicle for its process. TSMC thought of the chip not as a logic device but as a programmable fabric for detecting and diagnosing defects. TSMC then ran the full-FPGA mask set on each of the monthly process runs during development.

As the process neared completion and the Stratix IV neared initial tapeout, white-knuckles time arrived. "You had to be good with uncertainty," Cliff says.

Software and IP

The first team to jump on the FMT was the tool group—and with good reason. "We had software available to key customers a year before we had silicon," Chian says. "That was not long after we froze the process targets. So, we really had to trust those targets." It was particularly important, according to Altera's vice president of software and IP engineering, Udi Landen, for the tools team to understand the impact of the chip architecture on compilation times. "For big designs, compiles can run 24 hours," Landen says. "We are always working to reduce that time."

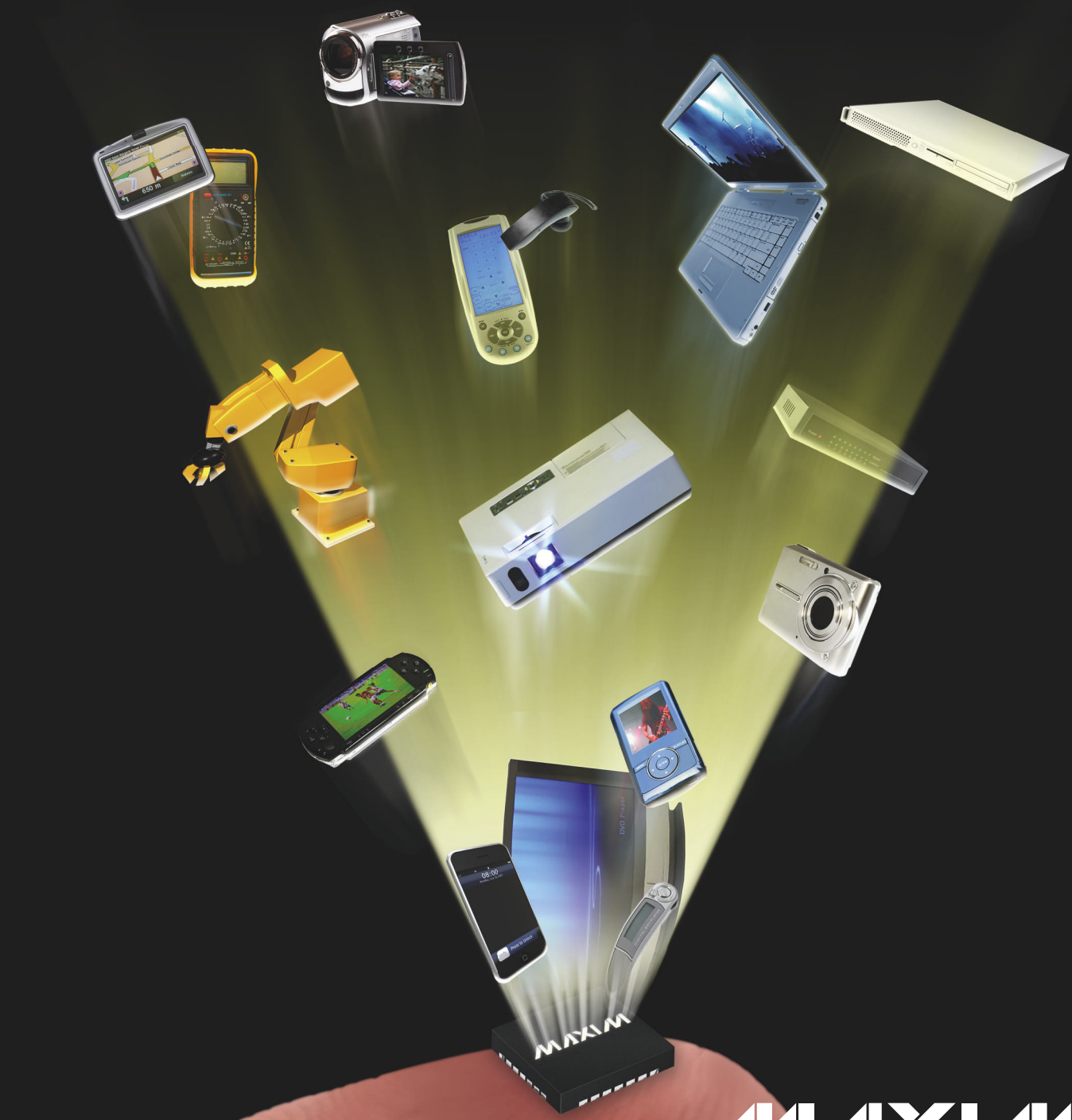
What might be less obvious is that IP development had to start early, as well, partially because some of the critical IP, such as the PCIe (peripheral-component-interconnect-express) Generation 2 core, had both hard-wired and programmable components. So Altera had to complete these blocks by the time that chip tapeout took place.

It was also vital to have the IP design process running in parallel because there was constant interplay between IP, chip, and process design. Early on, for instance, the team determined that the specification for the transceiver blocks was too limiting and that Altera would have to relax it. This change would influence how the highest-speed serial-interface standards would be implemented. Conversely, the performance requirements for PCIe Gen 2, the IP team found, implied that the embedded RAM in the controller block would have to run at 500 MHz. This parameter defined another requirement for the chip-design team.

All of this interaction required central supervision in the form of a program-management office, according to Landen. The office included representatives from each design group within the overall team and had a single program manager for each product family in the 40-nm process. There were more than 100 engineers at six sites worldwide, not including the people at TSMC, says Landen, so there had to be central coordination.

The Altera design illustrates an ambitious design collaboration. But any first adopter of a process node in this range will face similar complexity and risk. Perhaps the most important lessons here involve how Altera attacked that complexity—with centralized management of separate design tracks; designed, rather than accidental, communications links and decision points between the tracks; and an intentional change of the atmosphere between groups from adversarial to collaborative. These are no small achievements in themselves. ■

INNOVATION DELIVERED



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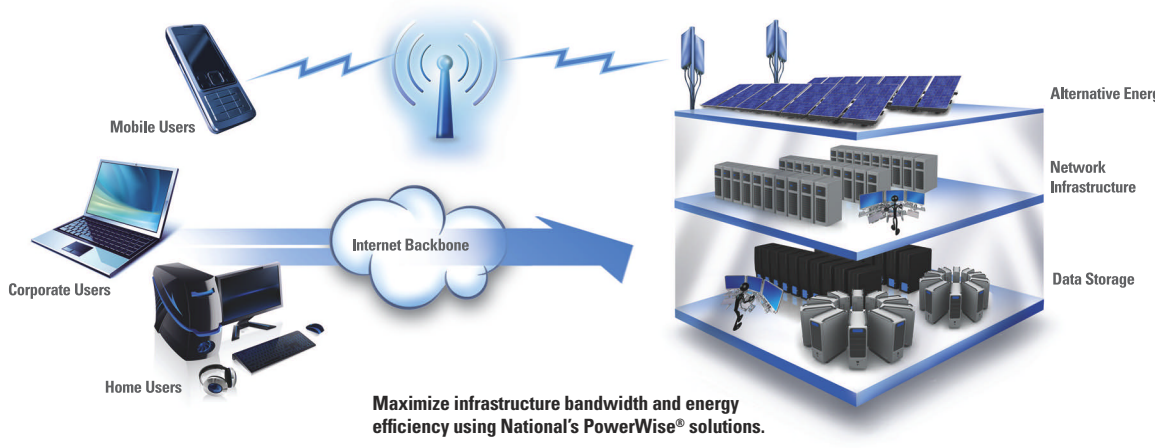

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Asset InterTech | GLENN WOPPMAN

Embedded instruments target product life cycle

EDN Innovator of the Year finalist Glenn Woppman describes technologies and partnerships that validate the embedded-instrumentation concept for chips, boards, and systems.

By Rick Nelson, *Editor-in-Chief*

EI (embedded instrumentation) shows promise for supporting design debugging, validation, and testing for chips, PCBs (printed-circuit boards), and systems, according to Glenn Woppman, president and chief executive officer of Asset InterTech. Woppman, a 2008 *EDN* Innovator of the Year finalist, last year scored several EI accomplishments as he positioned his company to help drive the emergence of EI through technology developments and partnerships with EDA companies and semiconductor manufacturers. He recently discussed Asset's history and 2008 accomplishments, sketched out a road map for 2009, and offered advice on how to facilitate innovation—whatever field you are in.

"We are really trying to make an impact over the entire life cycle of a chip, board, and system by reusing embedded instruments from chip design all the way through the system-integration phases and out into field service."

GLENN WOPPMAN
Asset InterTech

Woppman's work on what he describes as nonintrusive technology had its roots in the early 1990s, when he led a Texas Instruments team that contributed to the development of the IEEE 1149.1 boundary-scan standard. He then led the first employee spin-off in TI history, which gave birth to Asset InterTech in 1995, enabling the new independent company to offer its flagship ScanWorks boundary-scan tool to customers working with boundary-scan-compatible devices from multiple semiconductor manufacturers.

Boundary scan, which in its original incarnation provided shorts-and-opens testing as physical access disappeared, came into its own with the increasing popularity of BGA (ball-grid arrays) in the late '90s, which prevented physical test-probe access to buried solder balls. Boundary-scan tools continue to provide shorts-and-opens testing; the technology provides electrical access to buried nodes on dense PCBs through the IEEE 1149.1-defined TAP (test-access port). But the TAP, as Woppman and his counterparts at other companies realized, also provides a window into ICs that can serve uses ranging from in-system device programming to accessing internal embedded instruments.

Focusing on EI in '08

Woppman focused on this application in 2008, earning himself selection by *EDN* editors as one of four *EDN* Innovator of the Year finalists. The year didn't mark the company's first foray into the EI field; in 2004, Asset adapted its ScanWorks software to support Intel's IBIST (interconnect built-in self-test). But Woppman in 2008 repositioned his company to aggressively address the EI market. As part of the effort, he hired EI technologists from the Inovys operation of Verigy. He also established partnerships with EDA companies Mentor Graphics, Cadence Design Systems, and Synopsys, as well as with semiconductor makers Avago Technologies and Maxim Integrated Products.

Woppman attributes the need for EI in part to Moore's law: "Semiconductor

technologies are enabling new applications for consumers that never existed before, but, along with the applications come test and debug and validation challenges that weren't there before either," he says. "Our thrust has been to get a better understanding of the issues involved through participation in standards bodies such as the IEEE P1687 working group," which focuses on establishing a standard access mechanism for EI.

EI benefits extend well beyond chip debugging and testing. "We are really trying to make an impact over the entire life cycle of a chip, board, and system by reusing embedded instruments from chip design all the way through the system-integration phases and out into field service," he says. "We think embedded instrumentation has a huge value, and our customers and partners seem to think so, too, based on their participation in the P1687 group."

Woppman outlines key accomplishments for 2008: "On the semiconductor side, we were successful in proving out the I/O-instrumentation part of our vision by working with the Nehalem platform and QPI [QuickPath Interconnect] that Intel has developed," he says. Asset also developed and announced ScanWorks support for Avago Technologies' ASICs that incorporate QPI SERDES (serializer/deserializer) cores. Similarly, Asset adapted ScanWorks to support margining and forensics capabilities for several of Maxim Integrated Products' system-monitor and system-manager devices.

As for 2009, Woppman says, "We will continue to grow our partnerships on the semiconductor side with regard to I/O embedded instrumentation. In addition, we will begin to engage with our EDA partners and with customers around the core instruments initiative" based on the emerging 1687 standard. "Last year, we brought the concept of embedded-I/O instruments from belief to reality, and this year we want to turn the concept of core instruments from belief to reality," he says.

Fostering innovation

"If you look at technology companies, you'll find what I call the inside-out syndrome," says Woppman. "You've got smart engineers, who see a problem and go for a solution, and they often hit the mark, but sometimes the business case for their solution just isn't there." A better approach, he says, is an outside-in one, in which a company solicits input from the market before developing a technical solution to a problem.

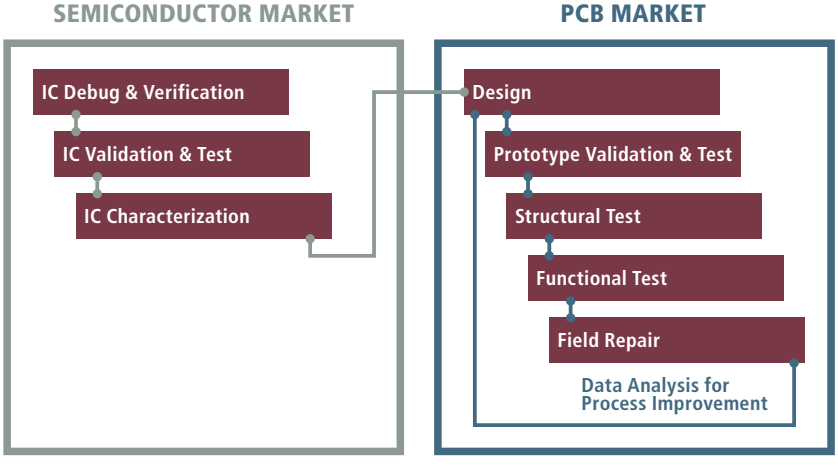
Woppman describes how the outside-in approach works at Asset. "One of our challenges was that we saw that the boundary-scan business was growing but wasn't going to be huge," he says. "So, we asked ourselves: How do we take our core competency and expand into other areas that could provide value for our current customers and attract new customers? We went through the process of really talking to a lot of different companies representing our customers and potential customers as well as our partners and potential partners."

Outside input, Woppman says, is necessary but not sufficient: "You've got to put some chips on the table. The Intel test director [Ashoke Seth] made a similar comment at Semicon West two years ago. He said that the IC ATE [automated-test-equipment] companies needed to place some bets on what the industry will need in the future. He noted that not all the bets are going to pay off for you but that you've got to put your chips on the table. And I think he was dead-on" (**Reference 1**).

Nevertheless, outside-in networking remains indispensable in helping to decide which bets to place. "You have to network and talk to a lot of people in the industry to try to figure out the trends you can exploit using your core competency," he says. "And you might identify trends that require a core competency you don't have, but you might be able to add that competency." Asset accomplished that goal in late 2007 when it acquired International Test Technologies to gain emulation expertise and in 2008 by hiring embedded-instrument experts.

EI convergence

Woppman sums up the innovation he's seen throughout the last year: "We've seen a convergence in this space among the different types of instrument IP [intellectual property], BIST IP, and so forth, all of which help the semiconductor side of the process through design simulation and on through IC-ATE test. Then, as the chip moves from the semiconductor production side to PCB assembly, embedded IP can be reused for functional tests, including microprocessor emulation or SERDES BER [bit-error-rate] testing. Of course, boundary scan still performs structural shorts-and-opens testing and is invaluable in improving yield in complex multiprocessor SOCs [systems on chips] and SIPs [systems in packages]. Ultimately, what we will see is an actual convergence of different test and instrumentation and debug capabilities within chips, within boards, and within systems that we'll be taking advantage of. The seed was planted with the IEEE 1149.1 boundary-scan initiative back in the early '90s, and now that seed has many trees, and those trees are growing." ■



Asset InterTech is aiming to use embedded-instrument technology to bridge the gap between chips and boards to facilitate full product-life-cycle support.

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1. Nelson, Rick, "Intel's Seth urges proactive test investment," Test & Measurement World*, July 10, 2007, www.tmworld.com/article/CA6458796.*

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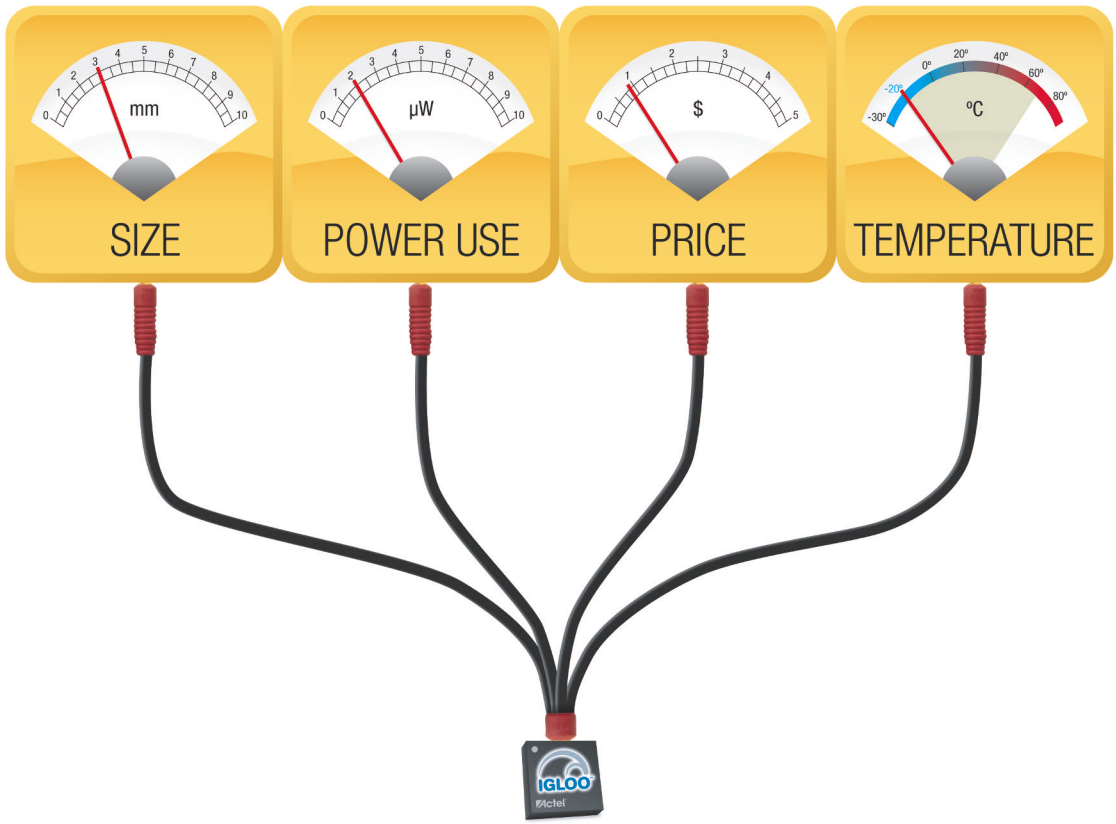

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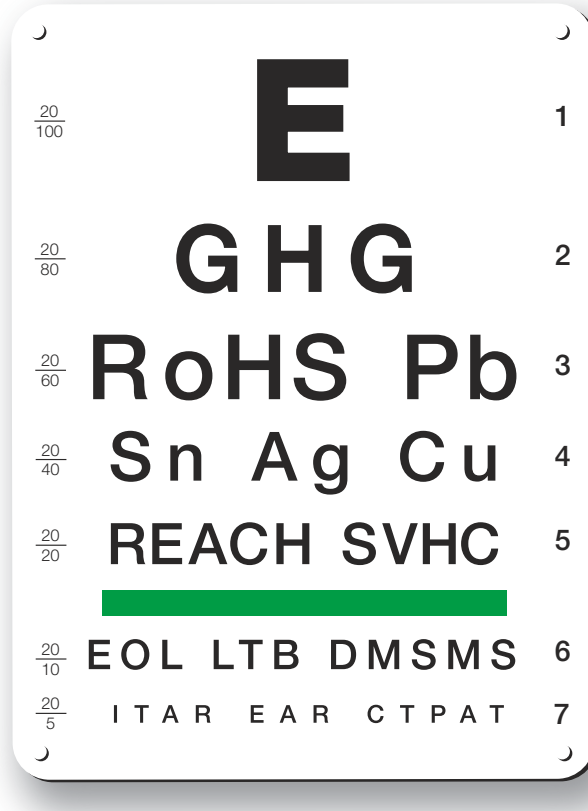

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A focus on reducing power consumption in DSPs

Octasic's Opus asynchronous architecture addresses power consumption for multicore DSP applications. **By Robert Cravotta,** *Technical Editor*

"The high end of the application space allows us to get our hands around all parts of the product."

DOUG MORRISSEY
OCTASIC

The Vocallo multicore media-gateway DSP is the first product employing the Opus core. *EDN* recently sat down and spoke with Tom Awad, Opus team leader; Doug Morrissey, chief technology officer and vice president; and Alain Legault, vice president of engineering, about the Opus engineering team. A portion of that interview follows.

What were the issues you were trying to solve when you started putting together the Opus architecture?

A key driving factor was that we wanted to achieve a performance and power ratio that was three times better than the current offerings. Another key factor was that we did not want to accomplish this ratio at the expense of the programming model. This was a multidisciplinary team effort where each part of the team had to work with and understand the issues of the other parts of the team. For example, the software guy had the responsibility to make sure that whatever we did maintained a standard [development] model to the customer in terms of how it ran. With a chip able to do low-channel versus high-density applications, we also wanted to introduce the concept of "pay as you grow," where we can enable additional codecs to be turned on in the future as the customer increases requirements.

What kind of design and implementation issues did you face, and how did you address them?

The nature of the problem we were trying to solve required input from all of the disciplines on the team. [Because it is asynchronous architecture], we had to develop some of our own tools to enable us to address the gate-level and silicon

Octasic's Opus engineering team included (left to right) Doug Morrissey, Tom Awad, and Alain Legault.

part of the design. In terms of integrating that with the architecture and into the software, we had to have our own compiler development, tools development, and debug environment to deal with the core. Developing a compiler and assembly language that both could implement C code efficiently and be implementable in an asynchronous architecture took quite a bit of interaction and a lot of cross-education so that both sides knew what needed to be done. I think that was a real team effort to make that happen.

On top of that, … while this is a great technology, a technology that cannot do anything is not worth too much, so we have a whole application that has been developed. Our first product offering includes [technology] all the way up to an entire application to work on a multicore DSP, which is the Vocallo gateway product. We are also working on other applications to go onto this and leverage the entire product platform.

We used our application team to validate the architecture as we went. The application team was developing the application even before everything was set in silicon. It was playing with the various paths we went down. We actually explored several paths as a team. Part of the decision of which was the right way to go was driven by schedule: When do you have to be complete? At some point, you have to be able to say it is good enough and move on. Each division of the team brought its own matters into the fray. In the end, everyone understood the other person's point of view and position, and we made a decision that this is the right time to freeze this portion of the design and move on.

Supporting the pay-as-you-grow concept requires a team effort because the way that is implemented is through software licensing. It involves everything from having nonvolatile RAM on the devices that needs to be configured during the manufacturing process all the way through the ordering system. So that what is delivered to the customer is actually a combination of silicon, a license file, and code licensing that is tailored to what the customer needs and can be upgraded over time.

There is quite a large software application just in that order process that manages the database and manages the configuration and needs to know everything about the software application and the hardware, and they all had to be designed with this model in mind. We have a guy on the team doing Web business-to-business programming, so when a customer places an order on the Web, it goes down to cutting an encrypted key to the DSP nonvolatile memory.

What was the processing sweet spot you were trying for with your architecture?

We are a multicore product, and, as a small company, we look at the high end of the market place as an easier place for us to differentiate ourselves. As you move down the performance-application curve, it becomes much more of an integration effort. The high end of the application space allows us to get our hands around all parts of the product—be that at the gateway-application level and all the way down to the silicon. So, from that perspective, we're multicore. One of the values we bring is that of being low-power. One of the limiting conditions of multicore is: How many cores can you stick on the die because of the power consumption?

One of the requirements that we had was that a single core must have a high enough level of processing performance to be useful to the traditional [programming] paradigm. There are a lot of multicore people out there that are looking at really tiny cores that you have to rethink your whole application, your whole problem, in order to use that device. So, our single core must have a minimum threshold of performance. There is an argument where that number lies, but it is significant.

The other aspect is: How many cores can I stick on a device that will optimally position the product for the widest application or end-product space that we can? We tried to target from a cost or die-size perspective something that would allow us to address the wide range of end-application space cost-effectively. We ended up with 15 cores [in our first product] that allowed us to address the high-end applications and still be cost-effective to go down to what would be considered the lower end of performance. We felt that the [number of cores] was the right mix to address the range of products we were looking to address. In the gateway product, that [approach] allows us to go from as low as eight to 16 channels to as high as 350 channels. If you look at the current products on the market, that range of performance would be divided into multiple silicon offerings, simply because the architecture does not lend itself to be cost-effective at the 16-channel space.

How do you preserve the traditional programming model with your multicore offering?

The biggest challenge with the asynchronous architecture and the compiler and getting all to work well together is branching. Any kind of branching in the code that changes the execution order, however that occurs, via a jump or some sort of test, causes challenges in asynchronous architectures. You are breaking the anticipated flow, and a normal assumption when you are architecting a core is that you are going to go from Address 1 to Address 2 to Address 3 and so on. Anytime you have a branch, for whatever reason, you're not going to execute Address 4 next; you're going to have to go somewhere else and start executing from there. In an asynchronous architecture, that is a synchronous event, so to speak, with the code execution. The instructions themselves, as long as you're doing them in order, [give] you no feedback that you have to react instantaneously to. It's a problem in synchronous designs, as well, but it produces some other, unique challenges in the asynchronous world.

As the team examined the implications to traditional compiler technologies and traditional assembly instructions, we were able to develop some unique execution-control-flow instructions or methodologies that the compiler was able to incorporate and allow us to avoid unnecessary branching in a way that people had not come across before.

We have a full ANSI C compiler. There are pragmas to help with optimization choices for the compiler. One of the interesting things is that the assembly is highly C structured. The assembly is inline with the C, but it is not just inline assembly; the C constructs flow into the assembly language. You can use any stack reference in the assembly instructions, as well as in the C instructions, and can flow back and forth between the two languages. The assembly supports all of the C typing. We have one semaphore to support the ability for cores to poke into the local register set of another core. ■

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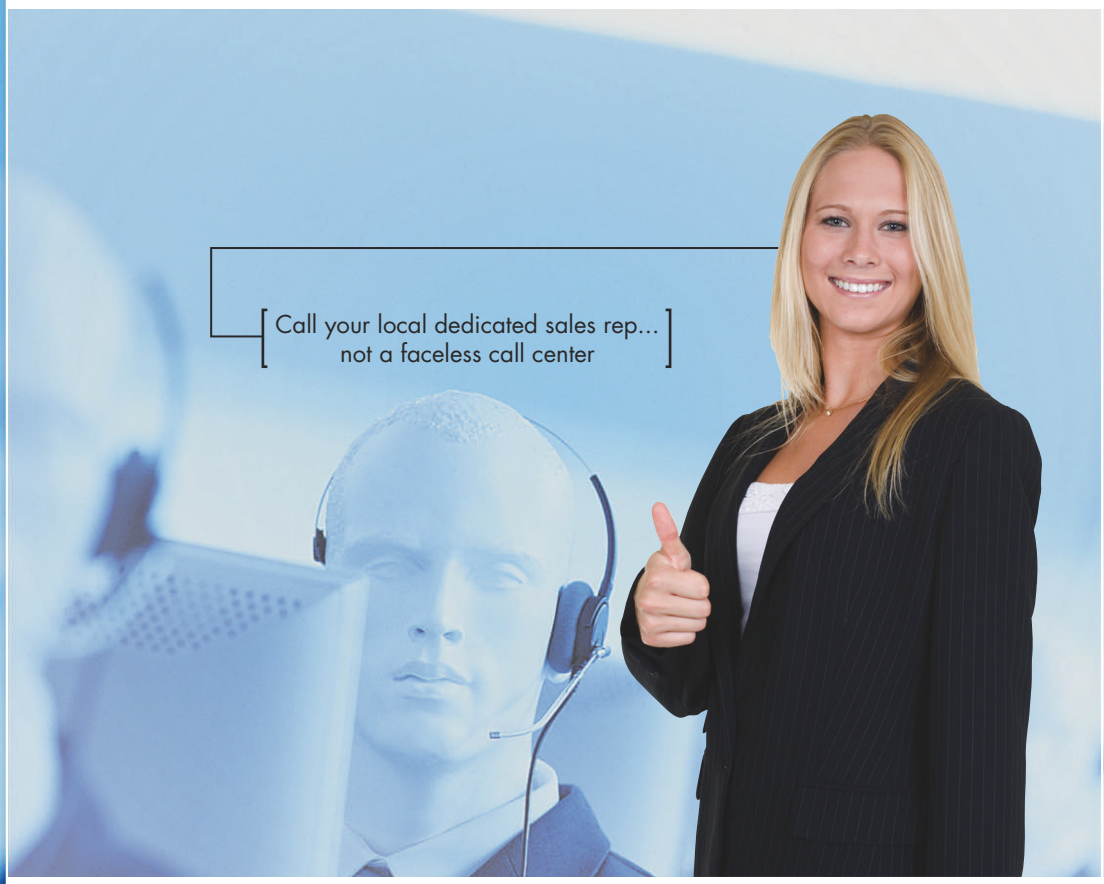

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SiGe Semiconductor | DESIGN TEAM

Teamwork makes challenging design task feasible

The SiGe team wanted to produce an RF-front-end module using the best technology for each component but still remaining cost-competitive with monolithic approaches.

By Ron Wilson, *Executive Editor*

"It was absolutely necessary for everyone to have a good understanding of the design requirements from the beginning."

BILL VAILLANCOURT
SiGe Semiconductor

Entering the market for IEEE 802.11n Wi-Fi hardware in 2008 might seem like a questionable proposition in a market teeming with announced and hinted entrants. Entering with a separate RF-front-end module in a market in love with integration might also seem strange. The design team from SiGe Semiconductor made those moves, however, and with some solid reasons. If the team could manage a challenging design to requirements and schedule, the company believed it would have an advantage. Thus was born the design effort for the SE2593A module.

The advantage was simple: no process compromises. To hit the emaciated cost points necessary for commodity 802.11n access points and terminal cards and still achieve a near-zero board footprint, vendors had been making hard choices: How do we minimize the number of semiconductor substrates? How do we achieve the lowest possible power? How do we slash the number of passive components? All of these questions have answers, but all usually mean compromises to performance.

A single-chip RF front end is certainly possible for an 802.11n radio, but each major component—the two power amplifiers at 2.4 and 5 GHz, the low-noise receiver amplifiers, the diplexers, and the transmitter/receiver switch—could ideally be in a different technology for optimum linearity, efficiency, and noise figures. Hence, any attempt to combine some of these components onto one die would risk performance compromises that might show up in field behavior.

SiGe's design team decided to take on a challenge: producing a module that uses the best technology for each component but still remains cost- and footprint-competitive with more monolithic approaches. It would mean simultaneously managing several chip designs using different models and tool sets, pulling all

The SiGe team included (left to right) Paul Huang, Chris Masse, Tony Quaglietta, Michael Goss, Joe Soricelli, and Mark Doherty. Also on the team were Craig Christmas, Ted Whittaker, Adrian Long, Gord Rabjohn, Bill Vaillancourt, Ed Pierce, and Peter Gammel.

the results together into a module, and somehow controlling the size and cost.

An architecture

In a way, differentiating by optimal process choices came naturally. As the company's name suggests, SiGe Semiconductor has deep experience in, and affinity for, processes other than vanilla CMOS. In fact, a SiGe (silicon-germanium) BiCMOS (bipolar-complementary-metal-oxide-semiconductor) chip would become the center of the module design, implementing both the 2.4-GHz power amp and the control circuitry that provided a serial interface to the baseband processor and programmable bias to the 5-GHz power amp.

"We wanted to get as much as we possibly could into the less expensive SiGe process," explains Bill Vaillancourt, senior director of the computer and home-electronics group at SiGe. "That meant creating the bias voltages for the A-band amplifier on the SiGe die and then passing them across to the A-band die." It also meant implementing the power detector for both amplifiers on the SiGe die.

The team chose to implement the A-band amplifier in GaAs (gallium arsenide) and selected a PHEMT (pseudomorphic-high-electron-mobility-transistor) process for the low-noise amplifiers, diplexers, and transmitter/receiver switch.

It was feasible to fit all three dice into a 5×6-mm package. But there was the small problem of the passive components for the transmitter filters and other signal conditioning. For those parts, the designers turned to yet another technology, IPDs (integrated passive devices). Three IPDs would be expensive but potentially less so than the discrete passives they would replace. The designers combined this technology with a substrate carrying the signal routing and some additional passives. The package vendor would bond the dice and IPDs to the substrate and then wire-bond the contacts on those devices to the substrate-interconnect pads. Die stacking was not used because the 1-mm height requirement for the module made stacking impractical.

A design flow

The design would require a cross-section of the company's resources, including teams in the United States, the United Kingdom, and Canada. Each chip design and the IPD work would require its own set of design tools and models. And the company's Hong Kong center, which manages assembly and test subcontractors, had to keep those teams in the loop, as well. Yet the company could not do the design in a piecemeal fashion. "We started from the pins of the module and worked our way in," says Vaillancourt. So, starting with the 50Ω signal connections and 3.3V supply, the design team proceeded to fill in the block diagram.

"It was absolutely necessary for everyone to have a good understanding of the design requirements from the beginning," Vaillancourt says. That foundation, plus regular meetings, frequent design reviews, and lots of conference calls, kept the three teams moving together. A specification doesn't cover everything, Vaillancourt points out. "You can't specify beforehand the isolation requirements on a die or the interactions between the transmit and receive chains. Everyone has to keep talking."

The key to the design process was extensive EM (electromagnetic) simulation. "We are used to having accurate EM models and simulating until the design is ready for tapeout," says Vaillancourt. "So, we applied that approach not only to the SiGe chip but also to all the chips." The continuous use of EM simulation was the best weapon the team had to control signal integrity. And, on such a dense module, signal integrity was a vital concern.

The team didn't just simulate the chips in isolation. "We never stopped cosimulation," says Chris Masse, the company's manager of module design. Working from the pins in, "the module design wrote the spec for the die designs. From there, we continuously refined the designs for the module, the dice, and the system in parallel."

SiGe had to do all of the detailed work for each die or IPD using the tool chain for that specific device. "It was a significant challenge working with different design kits and different tools for each technology," Masse observes. But all the information from the detailed simulations flowed into S-parameter models for system simulation. At the system level, the team applied both functional and Monte Carlo analysis using linear simulation. Masse says that the company decided against using harmonic-balance techniques because simulation would have taken too long.

Even at the mechanical level, simulation proceeded from abstract models to details. Only fine details, such as wire-bond lengths—which in the end would depend on the assembly subcontractor's equipment—had to remain empirical.

And the results

The multitrack design flow did converge. The only significant disruption to the flow was a change in specifications. "Right in the middle of the design, customers told us we would have to use a halogen-free substrate for the module," Vaillancourt says. So, the team had to resimulate the whole system with a new substrate material.

"Fortunately, that [task] meant only a small shift in the dielectric constant for the substrate," adds Masse. "It wasn't a matter of redesign so much as determining how much detuning the new material would cause and what that [detuning] would cost us in yield. We ended up touching a few of the traces to recenter the design a bit."

The largest unknown throughout the design was not even in the module; it was in the operating environment. "The typical Wi-Fi card is a horrible environment for RF," Vaillancourt observes. "In a MIMO [multiple-input/multiple-output] configuration, you need very linear behavior from your power amps at both full power and backed-off. ... You have to build in enough programmability to adapt to the uncertainties in the customer's design."

By providing programmable bias points and 50Ω connections to the outside world, the design team hoped to minimize the customer-support problem. And, if problem reports are a measure of success, the team seems to have succeeded on all fronts. "Customer boards came up very quickly with the sample modules," Vaillancourt reports. "With the sample board layouts, the data sheet, and the compliance matrices we are providing, we actually need very little applications-engineering engagement on our customer sites." ■

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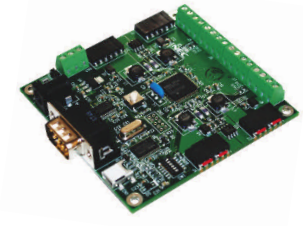

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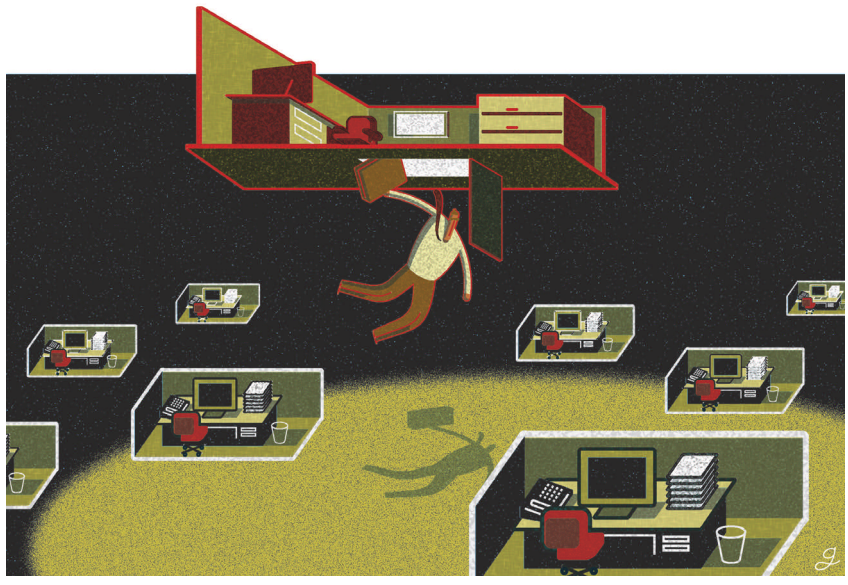


LIFE AFTER LAYOFFS

How to move forward after a job loss

With the number of job cuts continuing to rise and competition for open positions becoming more intense by the week, industry experts and career strategists share their advice on continuing an engineering career after being laid off.

By Suzanne Deffree,
Managing Editor, News

It's not fair, but it's a fact of life—or at least an engineer's life. Layoffs have been steadily on the rise since June 2008 and have soared since the fourth quarter in the semiconductor industry, with qualified, capable EEs receiving thousands of pink slips from Advanced Micro Devices, Fairchild Semiconductor, Intel, Motorola, and other companies. And, although the national unemployment rate increased to 7.2% in December, top technology state California saw its unemployment rate climb to 9.3% in the final month of the year, losing 78,200 more jobs and recording the largest month-over-month decrease in the level of employment among the states, according to data from the US Bureau of Labor Statistics. Statewide, more than 1.73 billion people were unemployed at the end of 2008.

"It's disappointing that the realities are that you can be doing a good job and do all the right things and it's like that old saying: 'No good deed goes unpunished,'" says Mike Demler, a former senior-staff product-marketing manger at Synopsys Inc (www.synopsys.com), who received his walking papers in late October and who as of mid-January was still unemployed. Employers can lay you off for reasons that have absolutely nothing to do with your job performance or even the condition of the company. "It's on my list of things they don't teach you in business school: how businesses are run and how decisions are made," he says. Demler's exit from Synopsys marked his fourth layoff since 1994 in a 32-year tech-industry career.

The current downsizing trend is an issue of great concern to IEEE-USA (www.ieee.org), one that the group projects will continue beyond 2009 and one that has encouraged it to gear up and advise its members on what services are available to help them make successful employment transitions. Part of that help will come through a survey of unemployed IEEE members in the United States, which found that employers are providing less in the way of severance, placement services, or retraining for laid-off workers than they did in the past. "Our survey also suggests that age is an increasing handicap in finding new employment, with each additional year of age adding about 3.5 weeks to the duration of unemployment," says Russell J Lefevre, IEEE-USA president.

It took Bill Betts, a 29-year industry veteran, 13 months to find a new job at Sun Microsystems Inc (www.sun.com) after suffering his first and only layoff from data-center-networking company Brocade in the fourth quarter of 2007. "It's difficult

to define, and it may be paranoia, but my age [was an issue while job hunting]," he says. "I'm 59, and, while you can scrub your résumé pretty cleanly, people can get a hint of how long you've been around. The skill sets in high tech quickly drop out of fashion. I think there's this perception that, the older you are, the less technical savvy you have. Also, the older you are, the larger the salary you typically have," he says.

Deb Dib, founder of Executive Power Brand (www.executivepowerbrand.com), a career-strategy consultancy, agrees. "There is still ageism out there," Dib says, advising that industry veterans show that they are aligned with what their younger counterparts are doing—knowing the latest design strategies, attending relevant conferences, or following pertinent blogs—and then show how their years of experience add to their own value proposition. "They have to prove that, even though they cost more, they are really a bargain because what they can produce is going to be so much more useful and perhaps happen faster or be more economical or more accurate," she says.

Kim Batson, founder of Career Management Coaching (www.careermanagementcoaching.com), a career-coaching and résumé-writing consultancy focusing on the tech sector, also maintains that industry vets can compete with lower-salaried newcomers. "If a company can see that a veteran candidate has something extra that they can bring to the table, they are more likely to pick the veteran over the grad," says Batson, a former recruiter for companies including Microsoft. "A veteran must show passion. All things being relatively equal as far as competency, the passionate candidate will win out the majority of the time," she says.

Veterans also must present themselves as flexible, strong, and articulate. Image and manners matter, she says, as do interview skills. "It's one thing to get in the door, but if they haven't interviewed in a long time, I suggest they get coaching from a professional on how to conduct a super interview, what companies are looking for, how to ask probing questions, how to work through the interview," Batson says, adding that the job seeker should look for professional help if necessary for creating job-hunting documents, such as a résumé and cover letter.

Further, veterans must be business-oriented. "It's not enough to be task-oriented and forget the business. Show a results-[driven] orientation. Everything they do needs to be tied to business results. Even if they are engineers, not necessarily managers, engineering a chip to go inside a laptop, they need to know how that innovation will affect the product, how the product will affect sales, and how sales will affect the company or productivity," she says. "They need to figure out what the impact of what they do is on the business. Companies are looking for that [skill] now, even among nonmanagerial staff. At the very least, it will help them stand out from the crowd."

> *"If a company can see that a veteran candidate has something extra that they can bring to the table, they are more likely to pick the veteran over the grad."*
>
> **KIM BATSON**
> Career Management Coaching

Both Dib and Batson specialize in personal branding, a career-coaching technique that encourages job seekers to find their own "sweet spot," or career niche, and then to communicate that niche as a value proposition to potential employers.

"One of the first things someone should do, apart from the mindset issues of adopting a future focus and avoiding an attitude of resentment about getting laid off, is to ascertain who they are and what they have to offer," says Batson. "That's what personal branding is all about: uncovering and articulating their value proposition to the market." (See **sidebar** "Advice for surviving job loss.")

Get online

Beyond that advice, job seekers should immediately tap their network and remain in connection with it. In today's career environment, that connection means being online and attending events in person. "Networking has changed in that it has now expanded from human interaction, face to face or over the phone, to online social networking," says Dib. "It's not that the online social networking has replaced traditional social networking, but it has broadened it and supplements it." The big mistake people make with networking is to ask everyone they know for job leads, according to Dib. "That's the kiss of death. What they need to do—and this is going to sound crazy to someone who is out of work—is go into networking as a 'give-to-get' gig. It's all about service. It is about being useful to other people. Build your relationship, developing that bank account of goodwill so that when you need something you don't feel shy about asking. Even more than that, it's letting people get to know you in a way that you become top of mind when they hear of something."

According to Batson, 50 to 60% of people get their jobs through networking, and she teaches that an effective job-search strategy includes creating an online presence. "Keep it professional. Keep the personal stuff off of there," she says, concerning LinkedIn pages or personal Web sites, which should include keywords to grab recruiters' attentions. Prospective employers will Google most people before calling them in for interviews, she says, suggesting that job seekers should claim at least the first three pages of a name-based Google search.

"Engineers, especially, can establish themselves as experts in their field by writing some articles, submitting them to Web sites, getting some speaking gigs—anything that will strengthen the real estate that is taken up when their name is Googled," Batson says.

Betts picked up that knowledge along the way. In addition to establishing himself on sites such as LinkedIn, he began blogging to create an online presence and contributed to *EDN* for a period of his unemployment.

Demler, who, like Betts, worked as a

designer for many years before moving into management, has also established himself as a knowledgeable blogger. As part of his career strategy, Demler is continuing "Analog Insights" (synopsysoc.org/analoginsights), a blog he writes for Synopsys, and, after his layoff, he started an independent blog, "The World Is Analog" (the-world-is-analog.blogspot.com). "I'm finding right now that my blog helps a lot. To some extent, people already know me, and I've never met them," he says.

Although no one would call a layoff a positive thing, it can be a push in the right direction. Betts, for example, says that, in the long term, Brocade would not have been a good fit for him. "Inertia is the most powerful force in the universe," he says. "If they hadn't had laid me off, I might still be there and be unhappy. But … being laid off for 13 months with no job … was pretty nerve-racking."

Meanwhile, planning career changes is somewhat of a rarity. "If you think about most people's career paths, they have a kind of zigzag path and typically through no planning. They start in one thing, and in two or three years, an opportunity comes to them through somebody they know," Dib says. "People flip all the time, but mostly in reaction—someone seeing something and saying they'd be great for it. With layoffs, the same thing can happen, but it has to be self-driven."

Is anyone hiring?

Although they are few and far between, some companies are hiring. For example, Synaptics Inc (www.synaptics.com), a developer of human-interface products, is looking for engineers. The company had more than 25 positions in the United States and Asia-Pacific to fill as of January, but the competition is stiff. Jim Harrington, vice president of human resources at Synaptics, reports the company is receiving more than 600 fresh résumés each month and that it interviews more than 20 people for each position it fills.

Harrington says that the company is looking for both veterans and recent college grads and is focusing on using its own Web site, as well as the major job boards and employee referrals, for candidate recruitment. "We're being much more aggressive in social networking and areas of recruitment," he adds.

Tech-focused online-career hub Dice.com (www.dice.com) also featured about 2600 electrical-engineer job openings as of mid-January, down from the 2800 it had in late November. Outside California, which has the most open positions on Dice.com, Maryland, Texas, and New York were the top geographies by volume of open EE positions at the time, according to Tom Silver, chief marketing officer for the company. "In terms of new résumés added, it is increasing substantially, and that's been the case all year [2008]," Silver says. "The anxiety associated with the economy has been with us for a while, and tech professionals seemed to be ahead of the curve in terms of their concerns."

Silver reports that new résumés posted on Dice.com in the fourth quarter of last year grew 67% versus the same period of 2007. Meanwhile, overall job postings in December decreased 25%, and, in January, the job count slipped further—a decline of 35%. "Demand for electrical engineers in early 2008 had been running relatively flat year over year as measured by job postings on Dice," Silver says. "However, in the last quarter of 2008 and at the start of 2009, EE positions, along with all demand in general, shifted."

Silver notes that many jobs never get posted, so it is important to have your résumé in the database. "This [step] becomes particularly important in a downturn because companies that may be having layoffs on the one hand need to fill critical open positions on the other. They will use the database but don't want to be seen advertising open positions," he says.

With competition for jobs high and the value of engineers often underassessed, one has to ask why educated and experienced industry veterans stick with the tech sector. "Why do I stay in this business? I've enjoyed the second half of my career moving from engineering to the business side of things," Demler says. "It's just an unfortunate fact of life that everybody in engineering, semiconductor, EDA, whatever, needs to be aware of: This is not a profession where you are likely to stay in one position or one job for any length of time."

Regarding the economic situation's impact on job searches, Demler says, "It's going to be tough. ... It's too late now for people who aren't prepared. [A layoff is] going to happen at some point. You'll be extremely fortunate if it never does. And it'll probably happen more than once." ■

ADVICE FOR SURVIVING JOB LOSS

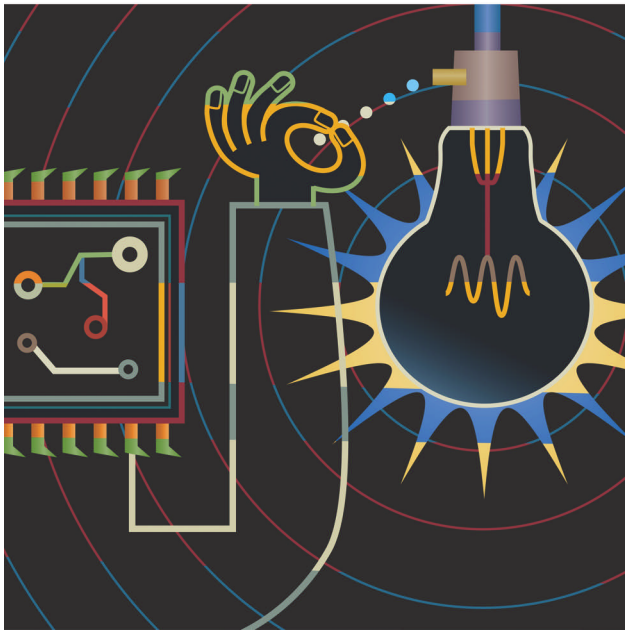
Career Management Coaching's Kim Batson offers the following points on how to survive and thrive after a layoff:

- **Accept your situation:** "These things happen to most people at least once in their careers," Batson says. "You may not know it yet, but it could be a blessing in disguise."
- **Adopt a future focus:** "Look forward, not back. View yourself as having a new job; your new job is to get a job, so you need to get going," she says.
- **Avoid resentment or self-pity about your current situation:** "Give yourself two to three days to process and grieve your loss," Batson says. "Then let go of all grievances; they only drain you."
- **Analyze your current financial situation** and sign up for unemployment if necessary.
- **Aim for a specific** functional, industrial, or geographical target.
- **Ascertain the value** that you bring to the marketplace or a potential employer by documenting your career accomplishments and creating a personal brand/value proposition.
- **Assemble a job search plan and documents,** including a résumé.
- **Act on your plan:** Take action in a structured, methodical manner, as you would with a full-time job.
- **Adopt a feeling of confidence:** "Act as if you are a rising star—even if you have been demoralized by a layoff or firing," Batson says.
- **Adjust your course if necessary:** Consider relocation, retooling, new certifications, or added education.

Endnote | RON WILSON, *Executive Editor*

It's time for innovation
to go beyond the technical

Our group was making money—how did I get laid off? It's a question a lot of engineers have to be asking right now. All over the industry, we see giant companies, such as IBM and Microsoft, announce great fourth-quarter and annual results and then follow up with a layoff announcement. We see smaller companies in the fabless world staying on track on product development, successfully offering samples to key customers and ramping revenue products—doing everything right—then suddenly making significant cutbacks, either laying off people or cutting back on projects that lead to layoffs elsewhere. And we see, if we look carefully, start-ups that are on track and meeting milestones just shutting their doors. What gives?



In part, it's because this recession is unlike any other in previous memory. This one started not with a sudden drop in demand, but with a global credit crisis. And, in many cases, the reason companies are laying off in the face of reasonably good operating results is not that they think demand will fall over a cliff—though the inability to deny that scenario is certainly a factor—but the fact that the credit crisis has continued to deepen and spread to the industrial economy. Lack of credit is no longer just the province of investment banks, insurance companies, and hedge funds; it's a fact in the world of real business.

Part of a chief financial officer's job is to make sure there is enough money to fund operations every month. In normal times, a company's business is cyclic. In some months, revenue more than covers operating-cash outflows. In other months, it doesn't, and the chief financial officer turns to cash reserves, short-term investments, or the company's credit lines. In the cases of companies with a limited range of products and long development cycles, these credit-funded shortfalls can last for a year or more.

Today, many companies have had their credit lines frozen, leaving the chief financial officer facing a grim situation. Absent the alternative of borrowing money, the company must have enough cash on hand to see it through a bad period. Because that requirement is much more conservative than it was just last year, most companies do not have enough short-term assets on hand to see them through at their current levels of fixed expenses. And, with forecasts falling, they are not likely to accumulate piles of cash this quarter, either. So, the only degree of freedom left is to cancel discretionary expenditures, delay the delayable, and reduce fixed expenses. That last part includes you and me. So, we see companies that are operating at a profit cutting costs like crazy—making a dead zone in the local economy around them—and even laying off critical employees.

So, what to do? The most important thing is to understand your company's cash-flow scenarios and its alternatives. The next most important thing is for all the executives, including the chief financial officer, to consider nontraditional sources of funding. Some people have scored help from obscure contacts in the Middle East or China. But more likely sources are key customers. Sufficient bridge funding to keep cash flow above zero may be an insurmountable obstacle for a little fabless-semiconductor company but a small risk for the huge system OEMs to which the company is important. In fact, from the system OEM's point of view, ensuring survival of the supplier of a key component in a promising new product may be a good short-term investment in its own cash flow. And, in some cases, you can build a similar scenario for key suppliers: They may be richer and have an interest in your survival much larger than the cost of ensuring it.

Now is the time for lateral thinking, not for reflexive conservatism. But lateral thinking means unprecedented sharing of information among engineering, financial, and corporate management. And it means resisting that reflex to pull back when the unknown yawns before us. ■

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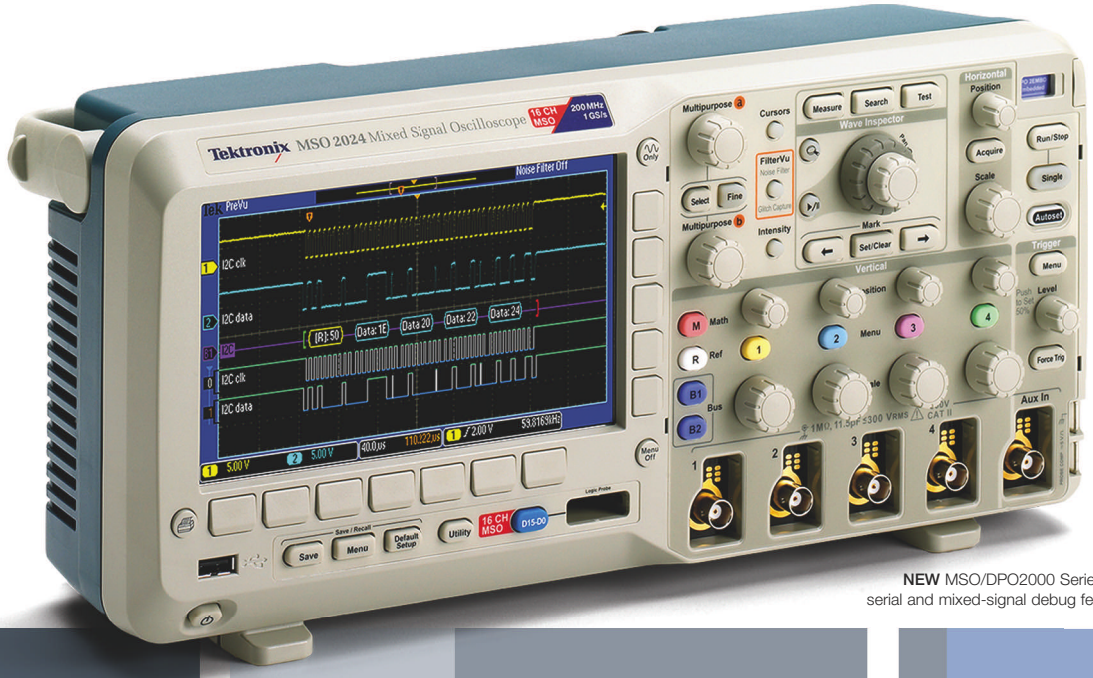

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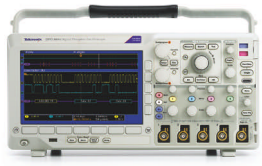

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READERS SOLVE DESIGN PROBLEMS

Buck converter uses low-side PWM IC

L Haachitaba Mweene, PhD, National Semiconductor Corp, Richardson, TX

The most common switching-power topology is a buck converter, which efficiently transforms high voltages to low voltages. **Figure 1** shows a typical buck converter in which the N-channel MOSFET, Q_1, needs a floating-gate drive signal. The floating-gate drive is part of the PWM (pulse-width-modulation) controller IC. Q_1 can be either N or P channel, depending on the controller's design. Unfortunately, the IC's voltage rating must be as high as the input voltage, which places a limit on the maximum voltage it can process.

The circuit in **Figure 2** uses a simple voltage-level shifter that lets a buck converter control a pass transistor with a low-side IC that has a ground-referenced gate drive. Because the level-shifting circuit in the PWM IC does not have to tolerate high voltages, you can implement a converter with an arbitrarily high input voltage.

PWM ICs with low-side gate drivers can power N-channel MOSFETs that are on when they have a positive gate-to-source voltage. The circuit in **Figure 2** uses a P-channel device as the high-side MOSFET; it's on when its gate-to-source voltage is negative. Therefore, you must invert the control signal from the PWM controller. A MOSFET totem-pole configuration comprising Q_2 and Q_3 will work, although you can also use an inverting-gate driver.

Capacitor C_2 performs the level-shifting. It must have a value large enough to maintain its charge at the switching frequency but small enough for its voltage to follow variations in the input voltage. Resistor R_1 and P-channel MOSFET Q_3 charge C_2 to a voltage of $V_C = V_{IN} - V_{CC}$, where V_C is C_2's voltage, V_{IN} is the input voltage, and V_{CC} is the supply voltage of the Q_2 and Q_3 totem-pole configuration and the PWM IC. The supply voltage must be less than zener diode D_2's breakdown voltage. Otherwise, current will flow through D_2 and C_2 whenever Q_2 is on, which lowers efficiency. D_2 limits C_2's voltage to the value in the above **equation**. When Q_3 is on, D_2 becomes forward-biased if the voltage attempts to increase. This circuit applies a 0V voltage between Q_1's gate and source when Q_3 is on, and it applies $-V_{CC}$ when Q_2 is on.

Resistor R_1 also ensures that Q_1's gate-to-source capacitance discharges, which keeps Q_1 off when the totem pole's output

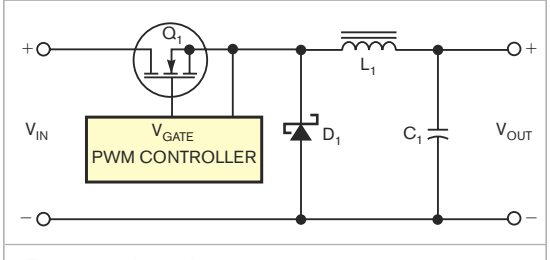

Figure 1 A basic buck converter uses a PWM controller and a MOSFET.

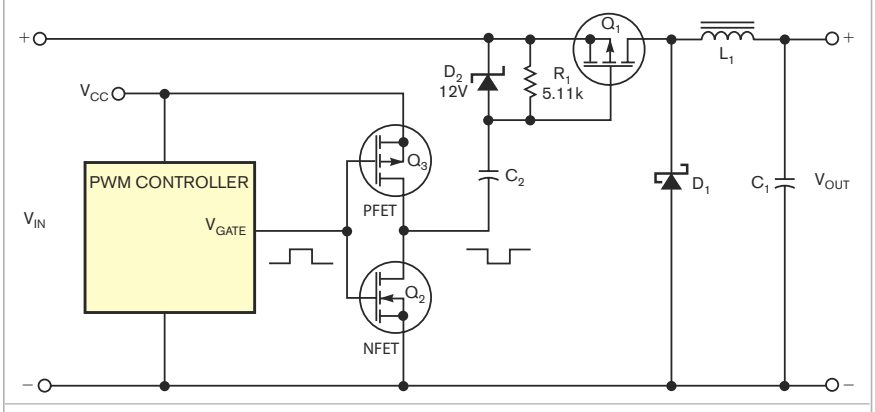

Figure 2 A level-shifting circuit provides low-side control of a buck converter's high-side FET.

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voltage is high. Diode D_2 limits Q_1's gate-to-source voltage to 12V regardless of the circuit's input voltage. Capacitor C_2 is transparent to Q_1's gate-drive pulse, so the circuit's gate-driving capability is just as good as that of the totem-pole circuit itself. The level shifting, therefore, imposes no limitation on the size of the MOSFET that the circuit can drive.

Figure 3 shows a practical buck converter employing this scheme. The converter's input voltage is 18 to 45V, and its output voltage is 12V at a 1.5A output current. The converter uses National Semiconductor's (www.national.com) LM5020-1 flyback/boost/forward/SEPIC (single-ended-primary-inductance-converter) PWM-controller IC.

The **figure** retains the component designators from the previous **figures** but adds functions such as input-voltage filtering in C_9; input-undervoltage lockout in R_2 and R_7; soft-start capability in C_3; switching-frequency-setting ability in 12.7-kΩ R_3 for 500 kHz; feedback compensation in C_7, C_8, and R_6; and output-voltage setting in R_9 and R_{10}.

The LM5020-1 provides current-mode control, but, in this circuit, it implements voltage-mode control. An internal sawtooth-current source with a peak value of 50 µA, which adds slope compensation to a current signal, serves as a voltage ramp. This current flows through 5.11-kΩ resistor R_4 and an internal 2-kΩ resistor to generate a ramp with a peak-to-peak voltage of 50 µA×(2 kΩ+5.11 kΩ)≃300 mV at the CS pin, Pin 8. The COMP pin, Pin 3, compares this sawtooth to the output error voltage at the COMP pin, which generates the right duty-ratio signal for Q_1.

Figure 4 shows the circuit's switching waveforms. Oscilloscope channel 1 (bottom trace) shows the gate-drive signal that the LM5020-1 generates. Channel 2 (middle trace) shows the corresponding totem-pole output voltage. Channel 3 (top trace) shows the level-shifted totem-pole output voltage between the source and the gate of Q_1. The peak value of Q_1's gate-to-source voltage equals the input voltage, and its amplitude is about 8V, the value of the supply signal that the LM5020-1 internally generates. All the waveforms are clean and have short rise and fall times. The full-load efficiency of the circuit is 86 and 83% at input voltages of 18 and 45V, respectively. EDN

Figure 4 Voltage waveforms in the buck-converter circuit of Figure 3 show clean voltages with short rise and fall times.

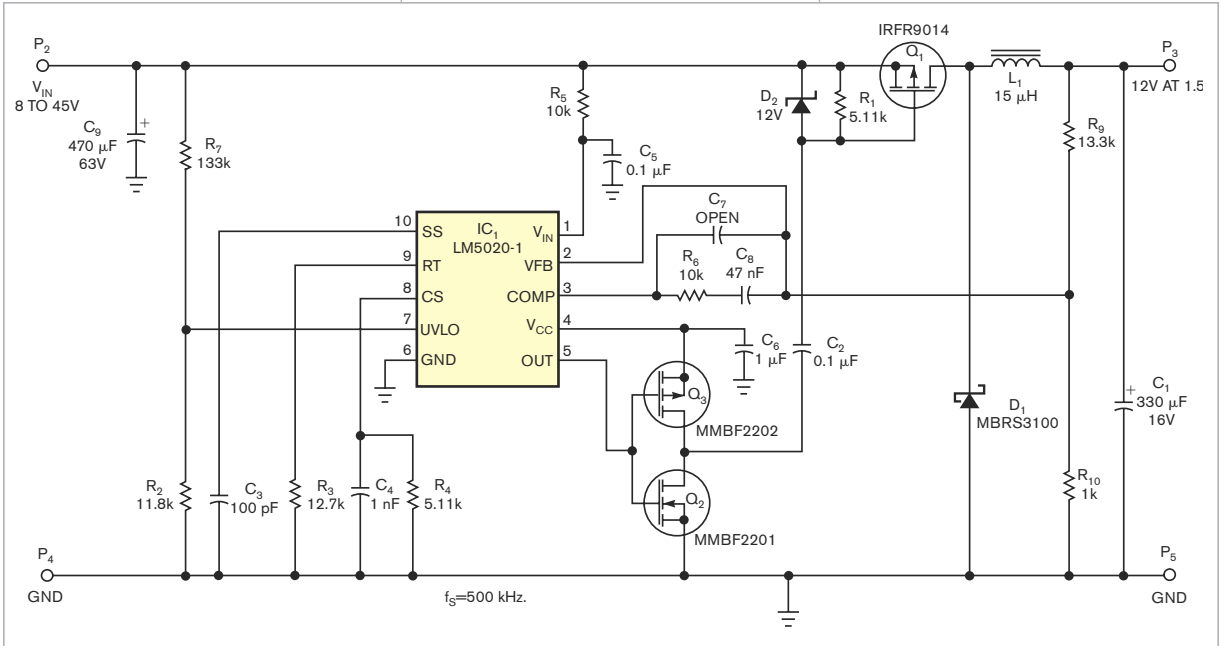


Figure 3 An alternative buck converter uses a low-side PWM IC to control MOSFET Q_1.

Isolated clock source acts as test generator

Daniele Danieli, Eurocom-Pro, Venice, Italy

Circuits such as PLL synthesizers, high-dynamic-range ADCs, and timing-sensitive digital networks require stable and spurious-free clocks. Testing these circuits is a difficult task when you use a master oscillator, even if the signal theoretically matches the application's phase noise and spurious responses. Variable clock-line loads, typical conditions in circuits under functional evaluation, and power-supply-line interferences, again typical in open-board environments on lab desktops, can degrade signal purity with jitter or unpredictable phase steps.

You can insulate an oscillator from a load requiring a special high reverse-attenuation-buffer stage, but it is more difficult to implement this insulation at frequencies of 10 MHz and more. This Design Idea describes a cost-effective approach to implementing an isolated clock source using a high-speed optocoupler with low input-to-output capacitance.

The circuit uses a quartz-oscillator stage with two NPN transistors in a conventional scheme (**Figure 1**). You select components C_3 and C_4 relative to the frequency; for 15- to 30-MHz frequencies, the corresponding values are 220 and 100 pF, respectively. You can scale up these values for lower frequencies. You can also substitute this stage with other equivalent circuits. A level-shift follower uses PNP transistor Q_3; a TTL-compatible signal at the output is available. You select resistor R_7 for the best pulse response; a value of 22Ω is adequate for most applications; however, you can omit the resistor if necessary.

You now apply a logic-level signal to the input pin of a high-speed CMOS optocoupler, IC_2. This design uses an HCLP-7101 type that operates at frequencies as high as 40 MHz, but new devices, such as the HCPL-77xx in SMD packages, are fully compatible. These optocouplers have input-to-output capacitance of less than 1 pF, and they have separate supply pins. If you do not use common grounds, as in the **figure**, you establish an optimized ultralow-power coupling, which provides effective isolation from load conditions and EMI (electromagnetic interference) that otherwise might modulate the incoming signal.

Note that the left side of the circuit, comprising an oscillator and the input half of the optocoupler, uses a dedicated battery to obtain the 5V supply voltage. On the right side, comprising the output half of the optocoupler, all lines directly connect to the board under test with relatively long cables; thus, they cause no disadvantages in the oscillator stage. You can use any optocoupler of adequate bandwidth as long as you pay attention to the correct power-supply voltage and the logic-level compatibility of IC_2. EDN

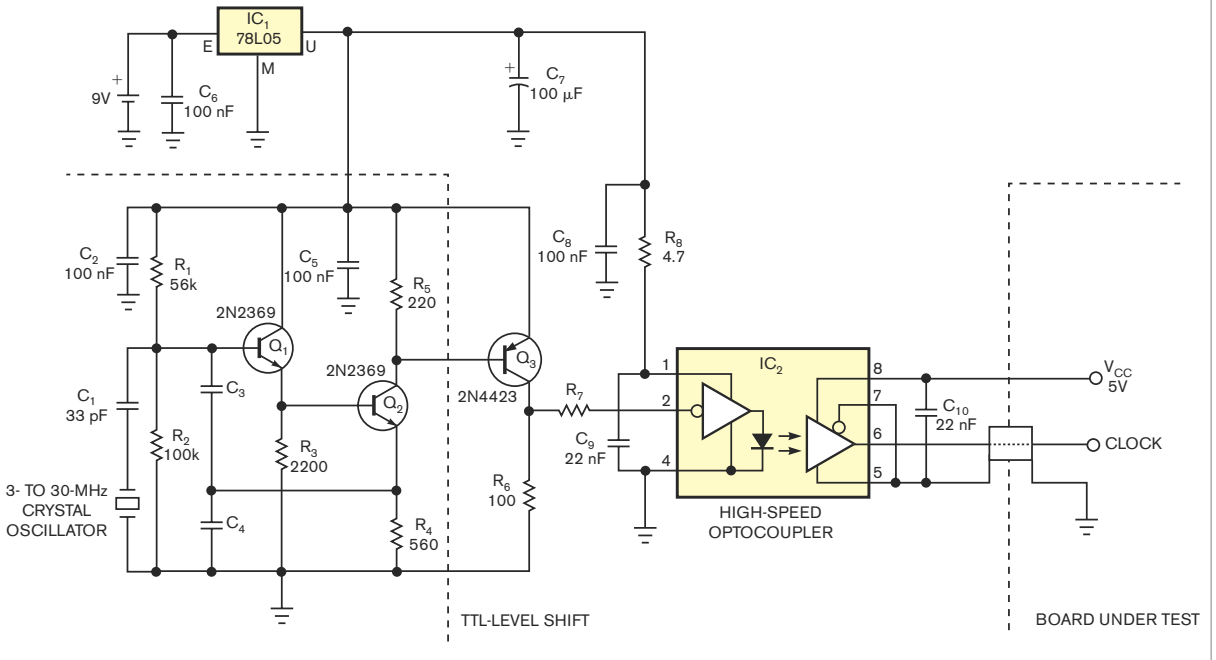


Figure 1 This circuit provides a cost-effective approach to implementing an isolated clock source using a high-speed optocoupler with low input-to-output capacitance.

Class AB inverting amp uses two floating-amplifier cells

Joseph Wee Ting, Institute of Atomic and Molecular Sciences, Sinica Academy, Taipei, Taiwan

Transistors often find use as three-pin amplifier devices, in which the input and the output share one pin. Thus, the input and the output must have the same voltage at this pin. On the other hand, a four-pin amplifier could isolate the circuit's input and output. Using optoisolators, you can design a four-pin Class AB amplifier. Although the output voltage of an optoisolator curtails its usefulness, you can add discrete transistors to form an isolated amplifier.

Figure 1 shows an example of a simple, 1-kV-p-p Class AB inverting amplifier that uses two identical floating-amplifier cells. The frequency response is dc to 20 kHz at full gain. You can achieve higher frequencies but at lower gains. The ratio of resistors R_2 and R_1 sets the gain. This circuit eliminates the need for many voltage-shifting components, which are typical of a standard circuit design. The positive and the negative cells are driven out of phase. The 15V and −15V and re-

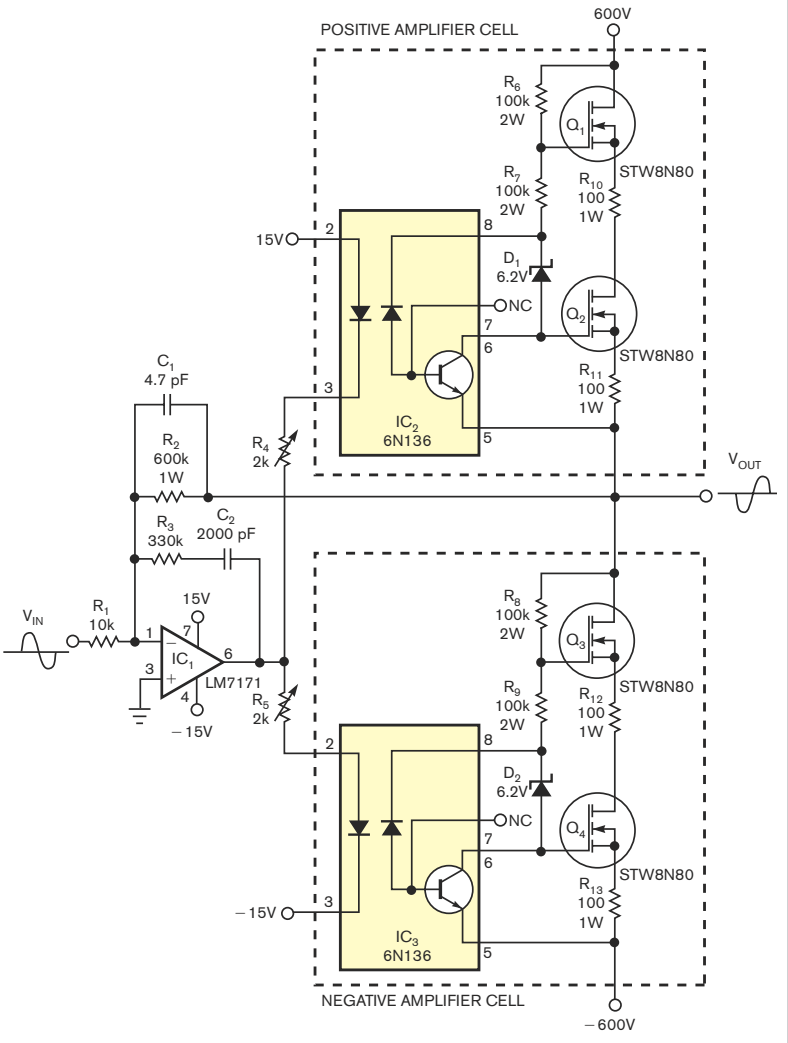


Figure 1 Transistors boost the output voltage and current of optoisolators, making an isolated amplifier output.

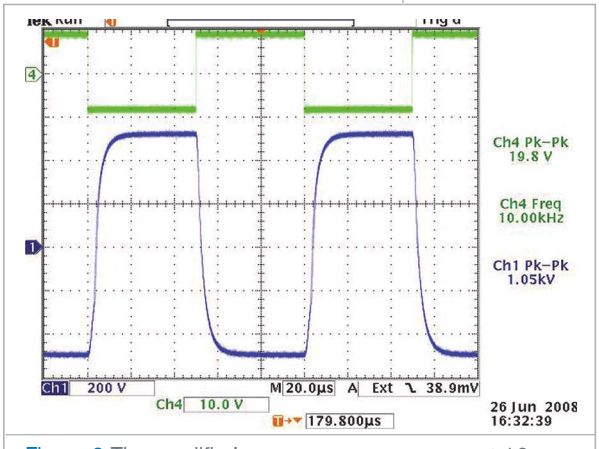


Figure 2 The amplifier's square-wave response at 10 kHz shows some high-frequency cutoff.

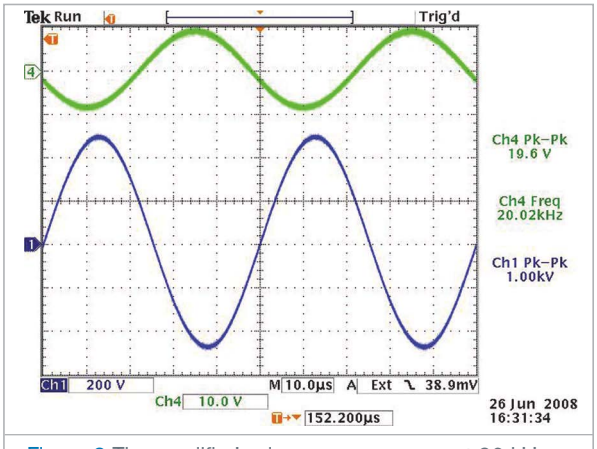
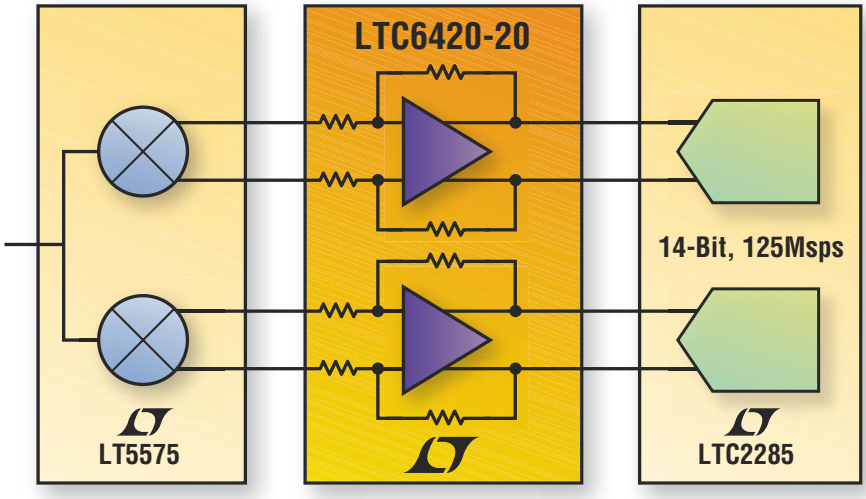


Figure 3 The amplifier's sine-wave response at 20 kHz shows a clean output signal.

Match to ±0.1dB, 0.1°



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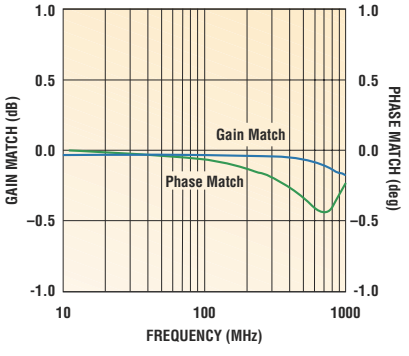
Channel-to-Channel Gain/Phase Match vs. Frequency



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sistors R_4 and R_5 provide the necessary bias to guarantee that the output transistors are always on. Careful trimming of R_4 and R_5 can remove the output crossover distortion. Zener diodes D_1 and D_2 keep the optoisolator photodiodes back-biased at 6.2V. Resistors R_{10}, R_{11}, R_{12}, and R_{13} supply some negative feedback to the output transistors. You must mount the four STW8N80 N-channel MOSFETs on suitable heat sinks to keep them cool. The circuit requires no active short-circuit protection. One pair of 125-mA currents across the high-voltage supply lines is sufficient to safeguard the circuit from destruction.

Figure 2 shows the square response at 10 kHz. There are no overshoots or undershoots, and the rising edge is almost antisymmetric with respect to the trailing edge. **Figure 3** shows the sine-wave response at 20 kHz. Both outputs are 1 kV p-p. EDN

DPGA conditions signals with negative time constant

W Stephen Woodward, Chapel Hill, NC

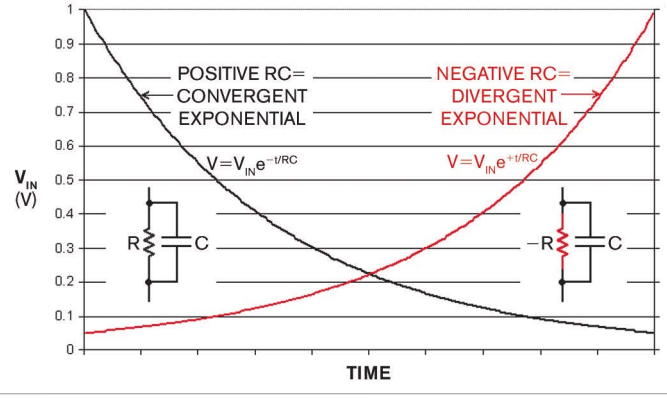

Figure 1 A negative time constant causes voltage to increase exponentially over time.

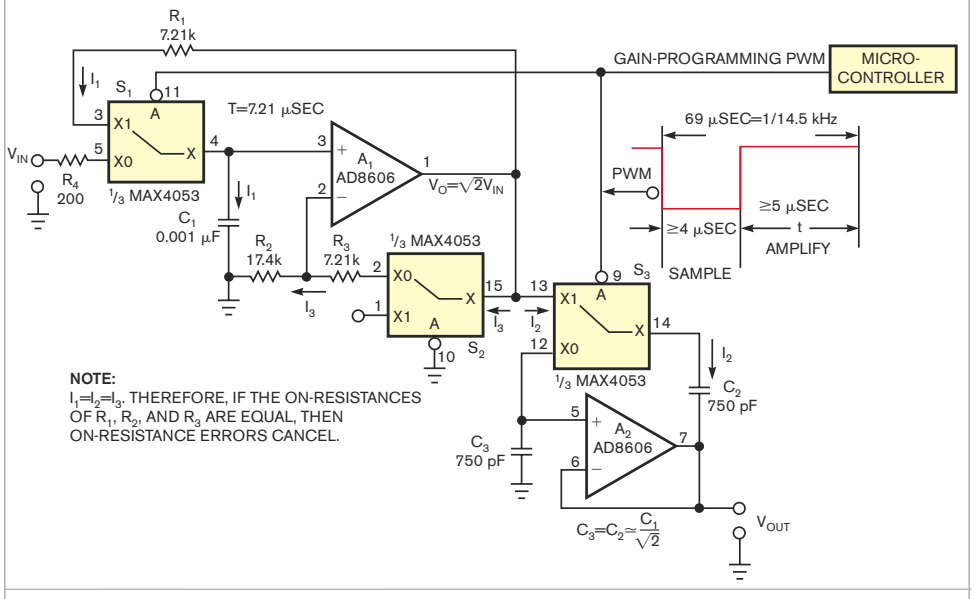

Figure 2 Positive feedback from amplifier A_1 causes C_1 to increase in voltage, which exponentially amplifies the input voltage.

DPGAs (digitally programmable-gain amplifiers) amplify or attenuate analog signals, which maximizes an ADC's dynamic range. Most monolithic DPGAs, such as the Linear Technology (www.linear.com) LTC6910 and the National Semiconductor (www.national.com) LPM8100, use a multiplying DAC in an op amp's feedback loop so that the DAC's input code sets the amplifier's closed-loop gain. Instead of using a monolithic DPGA, you can use two op amps and three analog switches to build a DPGA employing negative time constants.

You're no doubt familiar with the $e^{-t/RC}$ convergent exponential in which a capacitor in an RC circuit asymptotically discharges to zero. For input voltage, $V=V_{IN}/2$ at $t=T=\log_e(2)RC$, $V=V_{IN}/4$ at $t=2T$, $V=V_{IN}/8$ at $t=3T$, and so forth. Less familiar, but just as simple, is the behavior of the same RC topology when you replace R with an active circuit that synthesizes a negative resistance (**Figure 1**). If you replace resistor R with −R, you create a positive RC time constant. Thus, you create a divergent exponential, $V_{IN}e^{+t/RC}$.

Instead of converging to zero, the waveform theoretically diverges to infinity, and $V=2V_{IN}$ when $t=T$, $V=4V_{IN}$ at $t=2T$, $V=8V_{IN}$ at $t=3T$, and so forth. Therefore, you can amplify the in-

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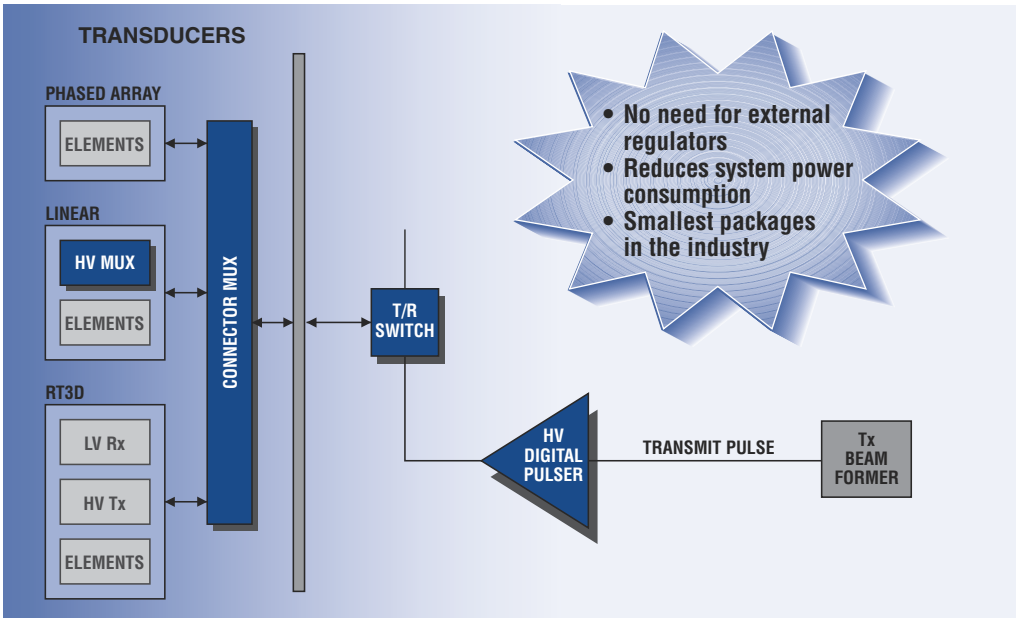

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put voltage by simply waiting the right amount of time ($t=\log_2(V/V_{IN})T$) after starting the negative discharge. The divergent exponential and the negative time constant are the core concepts of the circuit in **Figure 2**.

You can program the amplifier's gain with a PWM (pulse-width-modulation) signal from a microcontroller or another circuit. When the PWM signal goes to logic zero, sample-and-hold capacitor C_1 charges to V_{IN}. When the PWM signal cycles to logic one, op amp A_1 drives the R_1C_1 positive-feedback loop, creating a negative time constant. The resulting divergent exponential rise of C_1's charge continues as long as the PWM signal remains at logic one. That situation creates a net voltage gain of:

$$V_{OUT}(t)=V_{IN}2^{(t/10\ \mu sec+0.5)}.$$

THE NEAR-UBIQUITY OF PROGRAMMABLE-TIMER/COUNTER HARDWARE MAKES IT EASY TO DIGITALLY GENERATE A HIGHLY REPEATABLE PWM-CONTROL SIGNAL.

Thus, gain$=2^{(t/10\ \mu sec+0.5)}$ and log(gain)$=3+0.6$ dB/µsec. At the end of the amplification cycle, when PWM returns to logic zero, amplifier A_2 captures and holds the amplified input voltage.

The logarithmic relationship between gain and timing provides excellent gain resolution even when a PWM signal has just 8 bits of resolution and its programmable gain has a range greater than 0.2 dB/LSB step. (To view the log and linear plots of gain versus time using the amplify phase, go to the Web version of this Design Idea at www.edn.com/090319dia.)

The accuracy and repeatability of the timing of the exponential signal, the ADC sampling, the jitter, and the RC-time-constant stability all limit the amplifier's gain-programming accuracy. In **Figure 2**, 1 nsec of timing error, or jitter, produces 0.007% of gain-programming error. Fortunately, the near-ubiquity of programmable-timer/counter hardware in microcontrollers and data-acquisition systems usually makes it easy to digitally generate a highly repeatable PWM-control signal. EDN

Instrumentation amplifier compensates system offset from single supply

Luca Bruno, ITIS Hensemberger Monza, Lissone, Italy

Many integrated instrumentation amplifiers have architectures that permit offset compensation. The reference terminal's voltage, V_{REF}, adds in phase to the output to yield a gain of one. As a result, you can reset the output offset voltage by applying to the V_{REF} input a correction voltage of equal value but of opposite polarity. If the instrumentation amp operates from a dual-supply voltage, you can easily provide both positive- and negative-correction voltage. However, some instrumentation amps operate from a single supply—for example, in a battery-powered application—to amplify a signal source or a sensor that introduces a positive offset voltage. A sensor such as the AD590 from Analog Devices (www.analog.com), for example, produces an output current proportional to absolute temperature, and you should calibrate it at the lower reference temperature. In this case, the output swing of the instrumentation amp decreases, especially with high gain. To prevent this effect, you must apply a negative-correction voltage, which you generate from the positive power supply. In precision applications, the application of such a voltage may cause a problem.

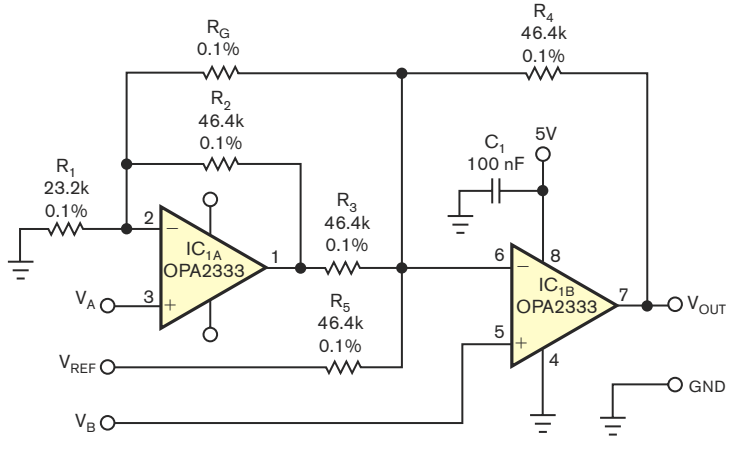

Figure 1 You can build an instrumentation amp operating from a single supply that permits you to reset the system offset by applying a positive-correction voltage to the V_{REF} input.

This Design Idea shows you how to build an instrumentation amp operating from a single supply that permits you to reset the system offset by applying a positive-correction voltage to the V_{REF} input. The circuit in **Figure 1** employs the dual high-precision OPA2333 op amp from Texas Instruments (www.ti.com). This op amp can

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	MAX7319–23	8	I²C	1.71 to 5.5	20	1.9	16 slave IDs
	MAX7324–27	16	I²C	1.71 to 5.5	20	1.9	16 slave IDs
	MAX6966/67	10	SPI	2.25 to 3.6	20	1.9	1.5% constant current, PWM
Now offered in CSP	**MAX6946**/47	10	I²C	2.25 to 3.6	20	1.5	1.5% constant current, PWM, **2mm x 2mm CSP**
	MAX7315	8	I²C	2 to 3.6	50	3.3	64 slave IDs, PWM
	MAX7316	10	I²C	2 to 3.6	50	3.3	64 slave IDs, PWM, $\overline{RST}$, INT
	MAX6964	18	I²C	2 to 3.6	50	3.3	4 slave IDs, PWM, blink
	MAX7300/01	20/28	I²C/SPI	2.5 to 5.5	10	11	16 slave IDs

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operate from a 1.8 to 5.5V supply and uses a proprietary autocalibration technique to simultaneously provide a maximum offset voltage of 10 µV and near-zero drift over time and temperature. It also offers high-impedance inputs that have a common-mode range 100 mV beyond the supply rails and rail-to-rail output that swings within 50 mV of the rails. Applying the superposition of the effects to the circuit in **Figure 1** yields the following **equation**:

$$V_O = V_B\left[\left(1+\frac{R_4}{R_3\|R_5\|R_G}\right)+\left(\frac{R_4}{R_3}\right)\left(\frac{R_2}{R_G}\right)\right]-V_A\left[\left(1+\frac{R_2}{R_1\|R_G}\right)\left(\frac{R_4}{R_3}\right)+\left(\frac{R_4}{R_G}\right)\right]-V_{REF}\left(\frac{R_4}{R_5}\right).$$

To achieve equal gain for both the V_B and the V_A inputs, resistors R_2, R_3, R_4, and R_5 must have equal values that are double the value of R_1. Using the resistor values in **Figure 1**, you obtain the following simplified **equation**:

$$V_O = \left(3+\frac{92.8\ k\Omega}{R_G}\right)(V_B-V_A)-V_{REF}.$$

The amplifier's differential gain is $3+(92.8\ k\Omega/R_G)$, and the reference voltage is added, inverted together with the output signal. Resistor R_G sets the gain, and, if you do not connect R_G, the gain assumes the minimum value, which is three; decreasing the value of R_G to 93Ω increases the gain to 1000.

The V_{REF} input requires a low-impedance connection to preserve a good CMRR (common-mode-rejection ratio); otherwise, you can use an op-amp buffer for better CMRR, which depends mainly on resistor-ratio matching. In this implementation, to preserve an acceptable CMRR, you must use precision film resistors. Analyzing the circuit, you can calculate the worst-case CMRR at low frequency. With R_2, R_3, R_4, and R_5 all of equal value and double that of R_1 and with all the resistors having equal tolerance, you obtain:

$$CMRR = \frac{3+\frac{2R}{R_G}}{6\left(\frac{\Delta R}{R}\right)},$$

where ΔR/R is the resistor's tolerance. If the tolerance is 0.1% and with the minimum differential gain, which is three, you obtain a CMRR of at least 54 dB. With a differential gain of 100, you obtain a CMRR of at least 84 dB.

The V_{REF} input can reduce the system offset to the lower output-swing limit but does not reset it completely because, in that case, the output voltage would be unable to reach the single-supply ground. If you want instead to reset the output offset, you can subtract this value using an ADC with differential inputs (**Reference 1**).EDN

REFERENCE

1. Bruno, Luca, "Circuit compensates system offset of a load-cell-based balance," *EDN*, Aug 16, 2007, pg 71, www.edn.com/article/CA6466208.

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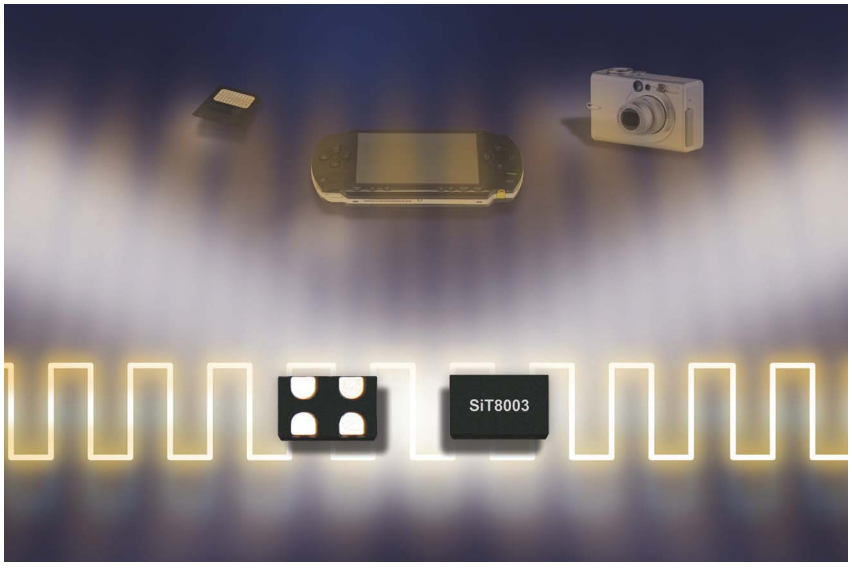

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SiTime Corp, www.sitime.com

Current-sense amplifier provides 1-µA supply current

The MAX9610 high-side, current-sense amplifier targets applications for monitoring USB ports and single-cell lithium-ion batteries in cell phones, PDAs, and other portable electronics. The amplifier features a 1.6 to 5.5V input common-mode range, a 1-µA supply current, a 0.5-mV maximum voltage offset, and a ±0.5% maximum gain error. The voltage-output device provides 25, 50, and 100V/V options. An external sense resistor allows you to set the maximum sense voltage at full-scale battery-load current. Available in 1×1.5×0.8-mm microDFP-6 and SC70-5 packages, the MAX9610 costs 64 cents (1000).

Maxim Integrated Products, www.maxim-ic.com

Amplifier front end provides high common-mode rejection

Providing a ±2.3 to ±18V power-supply range, the AD8295 integrated precision instrumentation-amplifier front end uses two uncommitted operational amplifiers and two precision-trimmed matched resistors. The device targets use in industrial-process controls, precision data-acquisition systems, medical-instrumentation equipment, and Wheatstone-bridge-measurement applications. Maintaining a minimum 80-dB to 8-kHz common-mode rejection for all grades at a gain of one, the device uses a resistor to set the gain from one to 1000. Using one resistor enables B-grade, 1-ppm/°C maximum gain drift, an 8-nV/$\sqrt{\text{Hz}}$ maximum input-voltage noise at 1 kHz, and 0.25-µV-p-p input noise at 0.1 to 10 Hz. Operating on single and dual supplies, the amplifier uses 2 mA of total current and has a −40 to +85°C temperature range. Available in a 4×4-mm chip-scale package, the AD8295 costs $2.89 (1000).

Analog Devices, www.analog.com

Differential-wideband amplifier features output-limiting clamp

Operating from a 29-mA supply current, the 900-MHz LMH6553 differential-wideband amplifier includes a programmable-output-limiting clamp for protecting ADCs and other downstream circuitry. Features include a supply range of 4.5V from a ±6V supply, 4-kV electrostatic discharge, 600-psec clamp-overdrive-recovery time and ±53-mV clamp accuracy. The amplifier also includes a 1.2-nV/$\sqrt{\text{Hz}}$ input-noise voltage, a 13.6-pA/$\sqrt{\text{Hz}}$ input-current noise, external gain-set resistors, and output common-mode control. A −40 to +125°C temperature range makes the device suitable for automotive-safety applications, including colli-

sion-avoidance, lane-departure, and backup-warning systems. Available in PSOP-8 and LLP packages, the LMH6553 differential amplifier costs $3.35 (1000).
National Semiconductor, www.national.com

1-GHz FET-input op amp combines low noise, high input impedance

Targeting use in medical diagnostic and portable devices, as well as instrumentation equipment, the single ADA4817-1 and the dual ADA4817-2 1-GHz FET input op amps combine unity-gain-stable and voltage-feedback amplifiers with FET inputs. The FET op amps achieve 4-nV/$\sqrt{Hz}$, 2.5-fA/$\sqrt{Hz}$ noise and high input impedance. Suiting photodiode preamps, the amplifiers provide 1.5-pF input capacitance; 2-mV maximum offset voltage; 1050-MHz, −3-dB bandwidth; and a 5 to 10V voltage range. The single ADA4817-1 comes in LFCSP-8 and SOIC-8 packages and costs $2.95 (1000); the double ADA4817-2 comes in an LFCSP-16 package and costs $4.98 (1000).

Analog Devices, www.analog.com

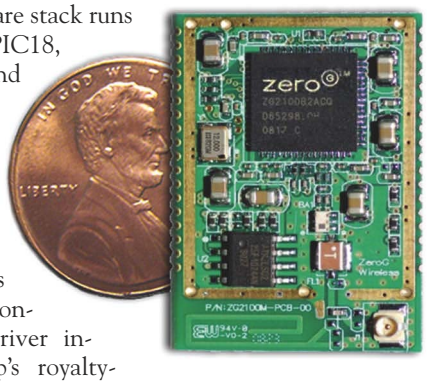
EMBEDDED SYSTEMS

Fanless computer comes in an industrial enclosure

Powered by Intel Core 2 Duo, Core Duo, or Celeron M processors, the PL-60590 compact, fanless computer uses Intel 945GME and ICH7R chip sets. The Intel 965GME chip set supports dual independent displays using CRT, DVI, and 24-bit LVDS technology, and the Intel 82573L Ethernet controller supports two GbE LAN ports. Features include four COM ports, six USB 2.0 ports, dual GbE ports, VGA, a PS/2 port, and an MIO module for expansion of I/O functions. The unit supports a 2.5-in. hard disk for high-capacity storage and a DDR2 533/667 DIMM socket for as much as 2 Gbytes of system memory. Available in an 8.7×8.5×3.5-in., rugged aluminum chassis, the PL-60590 costs $488.
Win Enterprises, www.win-enterprises.com

Kits add Wi-Fi to PIC microcontrollers

This series of Wi-Fi I/O-development kits for Microchip Technology's microcontrollers uses the standard PICtail and PICtail Plus daughterboard connectors, allowing designers to plug Wi-Fi connectivity into a variety of Microchip development kits. The PICtail daughterboard-based kits contain a ZeroG Wi-Fi module mounted to a PICtail daughterboard, along with software drivers. The ZeroG software stack runs on the 8-bit PIC18, 16-bit PIC24, and 32-bit PIC32 microcontrollers, as well as the dsPIC DSC families, requiring little additional system resources to add Wi-Fi connectivity. The driver includes Microchip's royalty-



productroundup

EMBEDDED SYSTEMS

free TCP/IP networking stack, so that customers who have used the stack can easily migrate from wired Ethernet to Wi-Fi communication. The module has an onboard antenna, with options for several external antennas. Prices start at $219.
ZeroG Wireless,
www.zerogwireless.com

Analog inputs have 2M-sample/sec throughput

The eight-channel MSXB080 signal-interface module features eight onboard ADCs and channel-to-channel isolation. Synchronizing to within a few nanoseconds of each other, each of the eight converters converts an analog signal to a 16-bit data stream at rates as fast as 250k samples/sec, providing a total throughput of 2M samples/sec. All of the inputs are differential, and each analog channel is isolated from other channels and any other system component. The modules cost $1395 each.
Microstar Laboratories,
www.mstarlabs.com

PCIe digital-I/O interface features optically isolated inputs

The DIO-32 PCIe digital-I/O-interface adapter provides 16 optically isolated inputs and 16 Reed-relay outputs. Isolated inputs protect PCs and sensitive equipment from voltage spikes and ground-loop currents in industrial environments. The socketed DIP resistors allow for configurable input ranges of 2 to 30V. The outputs provide long-life, dry-contact switch closures for low-current applications. Available in 3 to 13V or 10 to 30V inputs, the adapter costs $479.
Sealevel Systems, www.sealevel.com

INTEGRATED CIRCUITS

8-bit ADC family has low power consumption

The MAX19505, MAX19506, and MAX19507 pin-compatible family of dual-channel, 8-bit ADCs provides 65M, 100M, and 130M samples/sec and consumes 43, 57, and 74 mW of analog power per channel, respectively. Applications include power-sensitive, portable systems, such as ultrasound and medical imaging, portable instruments, and low-power data-acquisition systems. The ADCs provide a 49.8-dBFS SNR and a 69-dBc SFDR at 70 MHz. The devices include a self-sensing analog-supply regulator, allowing users to operate the parts from 1.8, 2.5, or 3.3V analog supplies with no external regulator. Additional features include single-ended or differential clock inputs, analog inputs with a 0.4 to 1.4V input common-mode range, and an onboard clock divider. Available in 7×7-mm TQFN-48 packages, the converters are pin- and feature-compatible with the 10-bit MAX19515, the MAX19516, and the MAX19517 ADCs. Operating over a −40 to +85°C temperature range, the ADCs cost $4.10 (1000).
Maxim Integrated Products,
www.maxim-ic.com

16-bit DAC comes in SC70 package

The single-channel DAC8411 DAC provides 80-µA operation at 1.8V, a 1.8 to 5.5V power-supply range, and a 6-µsec typical settling time. The 8- to 16-bit, pin-compatible device features a 17-mV power-on glitch and uses a three-wire serial inter-

INTEGRATED CIRCUITS

face, operating at clock rates as high as 50 MHz. Operating over a −40 to +125°C temperature range, the DAC has ±2 differential nonlinearity and ±8 integral nonlinearity. Available in an SC70 package, the DAC8411 costs $2.90.

Texas Instruments, www.ti.com

TEST AND MEASUREMENT

Universal counter provides 12 digits of frequency resolution

The Model 1105 universal counter integrates 12-digit frequency resolution and 40-psec time-interval resolution. The device provides built-in statistics and math-function options for analyzing display means, minimums/maximums, deltas, and standard deviations. Features include rise/fall time, period, phase, even counts, voltage-peak measurements, LAN control over Ethernet IP using a comprehensive GUI, and SCPI-command software. The Model 1105 costs $1765.

Berkeley Nucleonics, www.berkeleynucleonics.com

16-channel test module targets VPX systems

The 16-channel version of the vendor's SERDES test module plugs into VPX backplanes and directly tests channel compliance. Requiring no external equipment or special test fixtures, the device suits testing in VPX switches and node cards and backplane channels. The 16-channel SERDES test module costs $30,000.

Elma Bustronic, www.bustronic.com

EDN ADVERTISER INDEX

Company	Page
Advanced Interconnections	36
Agilent Technologies	41
	C-2
Analog Devices Inc	21, 23
austriamicrosystems AG	60
Cirrus Logic Inc	25
Coilcraft	9
Digi-Key Corp	1
EDN Magazine	C-3
	19
EMA Design Automation	42, 50
Ess Technology Inc	48
Express PCB	63
FTDI Ltd	32
International Rectifier Corp	7
Intersil	31, 33
	34, 35
Jameco Electronics	46
Keil Software	44
Lattice Semiconductor	15
Linear Technology Corp	17, 18, 55

Company	Page
Magna-Power Electronics Inc	49
MathWorks Inc	27
Maxim Integrated Products	57, 59
Mentor Graphics	37
Microsoft Corp	4
Mill Max Manufacturing Corp	11
Mouser Electronics	6
MTM Power Messtechnik Mellenbach GmbH	30
National Instruments	2
National Semiconductor	61
Pico Electronics	12
	45, 64
Samtec USA	10
Sealevel Systems Inc	43
Vicor Corp	28
Xilinx Inc	C-4

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BY GARRY MOTTER • SCIMEASURE ANALYTICAL SYSTEMS INC

Conspiracy theory

DANIEL VASCONCELLOS

My company was developing a system to drive a CCD (charge-coupled device) at the end of a long cable. This device required 12 separate clocks, swinging between approximately 5 and −10V, of various frequencies, phases, and duty cycles. We soon found that the ringing of these clocks on the far end of the cable was intolerable, so we added a resistive terminator to each line. We "barnacled" these terminators on the back of the prototype, and everything worked beautifully—at least enough for us to tweak the rest of the circuit.

Finally, it was time to re-spin the board, incorporating all the changes we had added to the prototype. Because the clock signals were fairly large, we used through-hole resistors for the terminators. When we powered up the system with the new revision of the board, the results were horrible. We couldn't get an image on the CCD at all, and the whole thing was "worse than dead." But it was a complicated system and a finicky CCD. My boss spent a couple of days fussing with the wave-generating and image-capturing software before concluding that the problem might be in the new board, and the problem landed back in my lap.

The first things to look at were the clocks. To get an accurate picture on the scope, I carefully attached the probe ground to the ground side of each terminating resistor before probing the hot side. Every clock was perfect, so I began to look elsewhere for the problem. I finally got a bit lazy with my scope, and, instead of grounding the probe at the optimal place for each signal, I just chose a central ground point and left it there.

The first clock worked beautifully, as did the second and the third. Sigh. But when I looked at the fourth one—whoa, Nelly! It was ringing so badly you couldn't tell where the rising edge was supposed to be. Continuing in this manner, I found that half of the clocks were good, but the others were lousy. I figured I'd better get a closer look and went back to my old method of grounding the probe on the resistor, and the ringing stopped. Eureka! The probe was providing the ground for the terminators but only one at a time—the one I was looking at. That action alone was not enough to change the symptoms of a badly behaving circuit. After I used a bit of wire and solder, the whole system was working like a charm.

I next had to find out why those six resistors weren't grounded. I had certainly designed them to be grounded. My CAD program showed that they connected to the internal ground plane in exactly the same way as the other six were. Then, I decided to look at the Gerber files with a third-party viewer. According to the Gerber files and in direct contradiction of the design, those six resistors were actually *not* connected to the ground plane. But one thing they had in common was that they were rotated from the default orientation.

Looking further, I found that my CAD program had an option to either draw or flash the pads. On this design I had somehow inadvertently selected the "flash" option. This program turned out to have a little bug that won't flash plane connections properly on a rotated pad. I had never previously thought much about flash versus draw, but it's now part of my checklist. One more thing to worry about: Your computer lies to you, and your oscilloscope covers up for it. **EDN**

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